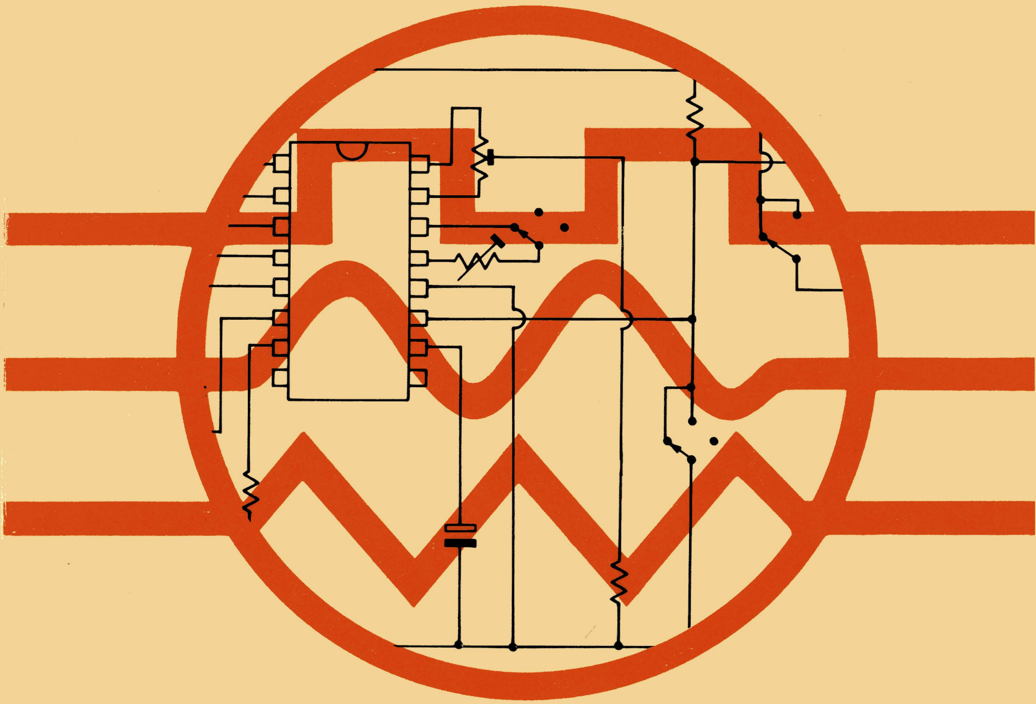
110 WAVEFORM GENERATOR PROJECTS FOR THE HOME CONSTRUCTOR



R.M.Marston

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R. M. MARSTON

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PREFACE

Waveform generators can be designed to produce outputs with sine, square, triangle, sawtooth, ramp, pulse, staircase or a variety of other forms. The generators may produce modulated or unmodulated outputs, and the outputs may be of single or multiple form. The generator circuits may be built using transistors, operational amplifiers or digital integrated circuits, or they may take the form of special-purpose waveform or 'function generator' integrated circuits.

In this book one hundred and ten useful waveform-generator circuits, of a variety of types, are presented. All the circuits have been designed, built and fully evaluated by the author. The operating principle of each circuit is explained in concise but comprehensive terms, and brief constructional notes are given where necessary. Like others in the '110 Projects' series, the book will be of equal interest to the amateur, the student and the professional engineer.

The outlines and pin notations of all semiconductors mentioned are given in Appendix 1, as an aid to construction: all these semiconductors are readily available types of American manufacture. Appendix 2 presents seven unique and useful waveform-generator design charts, as an aid to those readers who wish to design or modify waveform-generator circuits to their own specifications.

CONTENTS

CHAPTER 1

BASIC SINE-WAVE GENERATORS

The sine wave is the most fundamental and useful of all waveforms. Sine waves can be produced directly from suitable oscillators, or they can be synthesised or filtered from square or triangular waveforms. In this chapter we are primarily concerned with the direct generation of sine waves from basic oscillator circuits, although two special synthesiser circuits are shown and briefly described in the text. A total of fifteen useful sine-wave generator circuits are described.

C–R oscillator circuits

Two basic requirements must be fulfilled to produce a simple sine-wave oscillator, as shown in *Figure 1.1*. First, the output of an amplifying device (A_1) must be fed back to its input via a frequency-selective network (A_2) in such a way that the sum of the amplifier and feedback-network phase-shifts equals zero (or 360) degrees at the desired oscillation frequency, i.e. so that $x^\circ + y^\circ = 0^\circ$ (or 360°). Thus, if a transistor amplifier produces 180° of phase shift between input and output, an additional 180° of phase shift must be introduced by a frequency-selective network connected between input and output, in order to meet the first requirement of a sine-wave oscillator.

The second requirement of a sine-wave oscillator is that the gain of the amplifying device must exactly counter the loss or attenuation of the frequency-selective feedback network at the desired oscillation frequency, to give an overall system gain of precisely unity, e.g. $A_1 \times A_2 = 1$. It should be noted that if the system gain is less than unity, the circuit will fail to oscillate; if it is greater than unity the

system will be over-driven and the circuit will produce distorted (non-sinusoidal) waveforms.

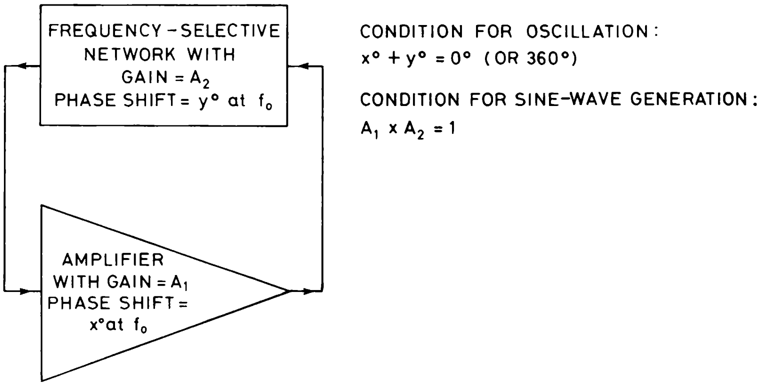


Fig. 1.1. Essential circuit and conditions of a sine-wave oscillator

The frequency-selective feedback network used in a sine-wave oscillator usually consists of either a *C–R* or an *L–C* filter network. *Figure 1.2a* shows the practical circuit of one of the crudest members

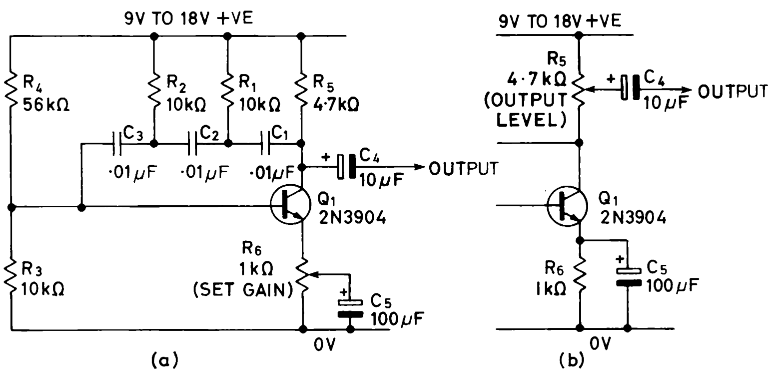


Fig. 1.2. 800 Hz phase-shift oscillator: (a) practical; (b) modified

of the sine-wave oscillator family, the so-called *phase-shift oscillator.*

Here, the output (collector) signal of the transistor amplifier is fed back to its input (base) via a three-stage *C–R* ladder network, essentially comprising C_1-R_1, C_2-R_2, and C_3-R_3. Each *C–R* stage of the ladder produces a phase shift between its input and output terminals. The magnitude of this phase shift depends on frequency and on the values

of the C–R components, and has a maximum value of 90°. The phase shift of the complete ladder network is equal to the sum of the phase shifts at each stage, and in the *Figure 1.2a* circuit (in which $C_1 = C_2 = C_3 = C$, and $R_1 = R_2 = R_3 = R$) equals 180 ° at a frequency of approximately $1/14CR$. Since the transistor stage itself produces a phase shift of 180°, the circuit actually oscillates at a frequency of roughly $1/14CR$. It should be noted that the three-stage ladder network has an attenuation factor of about 29 at the oscillation frequency, and that a high-gain transistor must be used in the Q_1 position to compensate for this high circuit loss.

In use, the *Figure 1.2a* circuit can be set up by carefully adjusting R_6 until the circuit just goes into oscillation. Under this condition the circuit produces a reasonably pure sine-wave output. In practice, oscillators of this type need frequent adjustment of the R_6 'gain' control if good sine-wave purity is to be maintained, since the circuit has no inherent gain stability.

The greatest advantage of the basic phase-shift oscillator is its cheapness, and its greatest defect is its lack of gain stability. With these points in mind, the circuit is often used simply as a crude and inexpensive fixed-frequency l.f. waveform generator, with its gain fixed at an excessive value so that a stable but moderately distorted sine wave is produced. *Figure 1.2b* shows a practical circuit of this type, in which the amplitude of the output signal is fully variable via R_5.

An alternative type of C–R sine-wave generator can be made by wiring a critically adjusted twin-T network between the output and the input of a suitable amplifier, as shown in the practical circuit of *Figure 1.3*. Here, a type 741 operational amplifier, wired in the inverting mode, is used as the amplifying device, and the twin-T network comprises $R_1-R_2-R_3-R_4$ and $C_1-C_2-C_3$.

In a normal twin-T circuit the network is said to be balanced when its components are in the precise ratios $R_1 = R_2 = 2(R_3 + R_4)$ and $C_1 = C_2 = C_3/2$. When the network is perfectly balanced it acts as a frequency-sensitive attenuator, and gives zero output at a centre frequency equal to $1/6.28R_1C_1$ (see *Figure 8.2 and 8.3* design charts), and a finite output at all other frequencies. When the network is imperfectly balanced it gives an attenuated but finite 'null' output at the centre frequency, and the phase relationship of this output signal depends on the direction of the imbalance. If the imbalance is caused by $(R_3 + R_4)$ being low in value, the output signal is 180° out of phase with the input at the null frequency; if $(R_3 + R_4)$ is high, the output signal is in phase with the input at the null frequency. It should be noted that a rapid change in phase relationship occurs in either case as the input signal sweeps through the null frequency.

Thus the twin-T network can be used as the basis of an oscillator in conjunction with either an inverting or a non-inverting amplifier, simply by connecting the network between the input and output of the amplifier and adjusting the value of $(R_3 + R_4)$ to give an output phase relationship and a 'nulled' gain factor that is compatible with the amplifier. Such a circuit has excellent frequency stability, because of the sharp phase sensitivity of the twin-T network at its 'null' frequency.

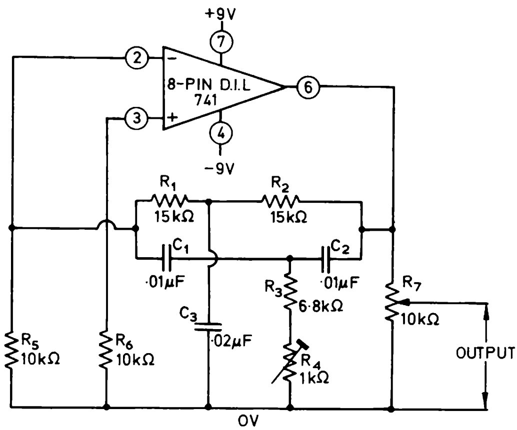


Fig. 1.3. 1 kHz twin-T test oscillator

The *Figure 1.3* twin-T circuit acts as an excellent fixed-frequency (1 kHz) test oscillator. The amplitude of its output signal is fully variable from zero to approximately 5 V r.m.s. via R_7. In use, R_4 should be adjusted so that the circuit only just oscillates, under which condition the output typically contains less than 1 per cent total harmonic distortion. Automatic amplitude control is obtained in this circuit because of the progressive non-linearity of the op-amp as its output signal approaches the clipping level.

An alternative method of automatic amplitude control is shown in the 1 kHz oscillator circuit of *Figure 1.4*. In this case silicon diode D_1 is wired between the input and the output of the op-amp via potential divider R_7. The diode progressively conducts and reduces the voltage gain of the amplifier circuit when the voltage across the diode exceeds a few hundred millivolts, and thus functions as an automatic amplitude control.

To set up the *Figure 1.4* circuit, first set R_7 so that its slider is at the op-amp output end of the pot. Now adjust R_4 so that oscillation is just sustained. Under this condition the sine-wave output signal has

an amplitude of about 500 mV peak-to-peak, or 170 mV r.m.s., and all adjustments are complete. R_7 then enables the output signal, which contains negligible distortion, to be varied between 170 mV and 3 V r.m.s.

The *Figure 1.3 and 1.4* circuits act as excellent fixed-frequency sine-wave generators, but are not recommended for variable-frequency

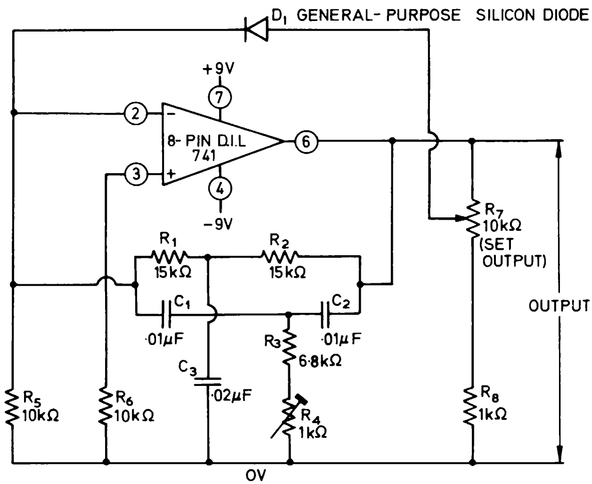


Fig. 1.4. Diode-regulated 1 kHz twin-T oscillator

use, because of the difficulties of varying three or four twin-T components simultaneously. An excellent variable-frequency sine-wave oscillator can, however, be made by using a Wien *C–R* frequency-selective feedback network in conjunction with a non-inverting amplifier, as shown in the 150 Hz to 1.5 kHz op-amp oscillator circuit of *Figure 1.5.*

Here, the Wien network comprises a series *C–R* network ($C_1-R_1-R_2$) and a parallel *C–R* network ($C_2-R_3-R_4$) connected in series. Input signals are applied between ground and the top of C_1, and output signals are taken from between ground and the top of C_2. The main feature of the Wien network is that the phase relationship of its output to input signal varies from –90° to +90°, and equals zero at a certain 'centre' frequency. Normally, as in the *Figure 1.5* circuit, the Wien network is symmetrical, so that $C_1 = C_2 = C$, and $R_1 + R_2 = R_3 + R_4 = R$, in which case the centre frequency is defined as $f = 1/6.28CR$; see *Figure 8.2 and 8.3* design charts. At this centre frequency the network has an attenuation factor of three.

Thus the symmetrical Wien network can be used as the basis of an oscillator by connecting a non-inverting amplifier with a gain equal to the Wien loss factor between its input and output. In the *Figure 1.5*

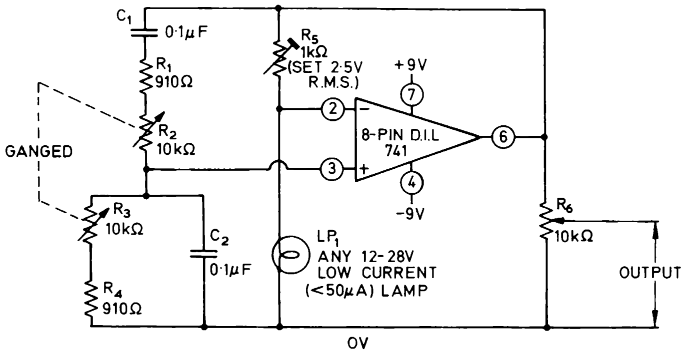


Fig. 1.5. 150 Hz to 1.5 kHz twin-T oscillator

circuit, automatic gain control is obtained by wiring R_5 and incandescent lamp LP_1 in series as a self-adjusting gain-setting potential divider, giving a nominal gain of three, across the op-amp. The lamp can be any 12 V to 28 V type with a current rating less than 50 mA. When the circuit is correctly set up, the sine-wave output signal typically contains about 0.1 per cent total harmonic distortion, and the circuit draws a total current of about 6 mA from the supply lines. The circuit is set up by simply adjusting R_5 to give approximately 2.5 V r.m.s. output at the maximum setting of R_6.

Figures 1.6 to 1.9 show some simple variations of the basic *Figure 1.5* Wien oscillator circuit. The *Figure 1.6 and 1.7* circuits rely on the onset of diode or zener diode conduction for automatic gain control. Both circuits inevitably produce a slightly (1 or 2 per cent) distorted waveform, but offer the great advantage of producing zero amplitude 'bounce' when range sweeping in variable-frequency circuits. The maximum peak-to-peak output of each circuit is roughly double the breakdown voltage of its semiconductor regulator element.

In the *Figure 1.6* circuit the diodes begin to conduct at 500 mV, so the circuit gives a maximum peak-to-peak output of only 1 V. In the *Figure 1.7* circuit, on the other hand, zener diodes ZD_1 and ZD_2 are connected back-to-back, and may have values as high as 5.6 V, so the maximum peak-to-peak output may be as high as 12 V or so. Each circuit is set up by adjusting its 'set gain' control to the maximum value at which oscillation is just maintained across the whole frequency band.

The frequency range of each circuit can be altered by changing its C_1 and C_2 values if desired. The maximum useful operating frequency of each circuit is limited to about 25 kHz, due to the slew-rate limitations of the 741 op-amp.

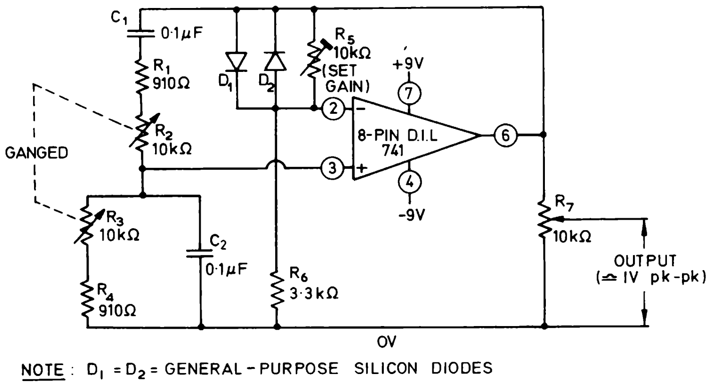


Fig. 1.6. Diode-regulated 150 Hz to 1.5 kHz Wien-bridge oscillator

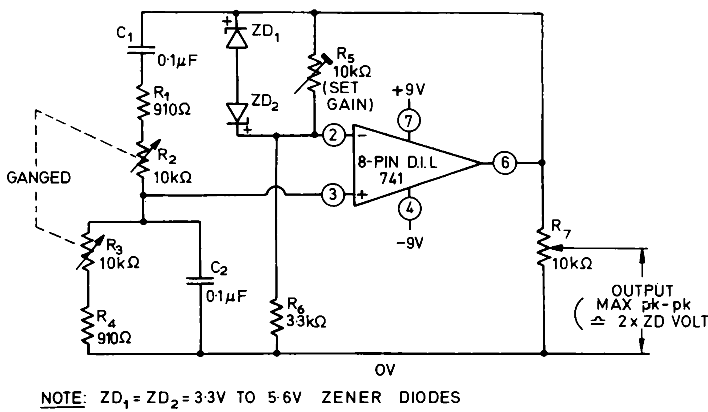


Fig. 1.7. Zener-regulated 150 Hz to 1.5 kHz Wien-bridge oscillator

Figure 1.8 shows the circuit of a fixed-frequency (1 kHz) Wien oscillator that uses only a single power supply for the op-amp. R_7 and R_8 act as a potential divider, to give a quiescent half-supply rail voltage, and C_3 bypasses R_8 to a.c. and thus gives an effective low-impedance supply path for the circuit. Normally, with R_3 and R_4 out of the circuit, oscillation occurs at slightly less than 1 kHz; R_3 and R_4 are used to

shunt the R_2 arm of the Wien network, and thus raise the operating frequency to precisely 1 kHz. If necessary, R_3 can be increased or decreased in value to bring the frequency to precisely 1 kHz if the tuning capacitors are substantially out of tolerance.

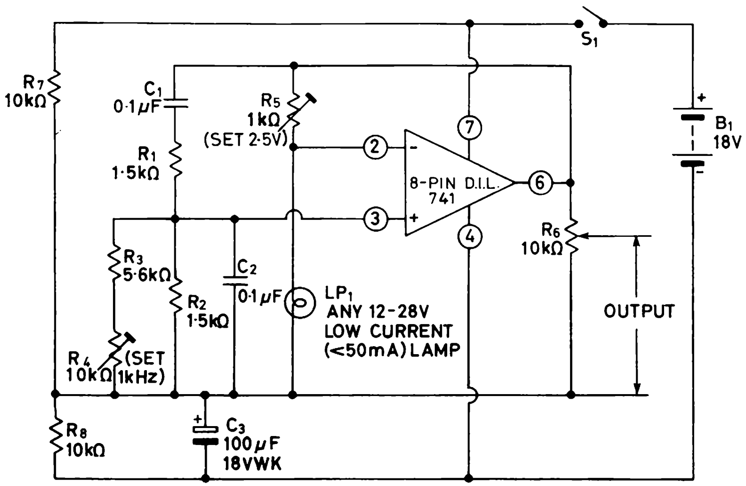


Fig. 1.8. Single-supply 1 kHz Wien-bridge oscillator

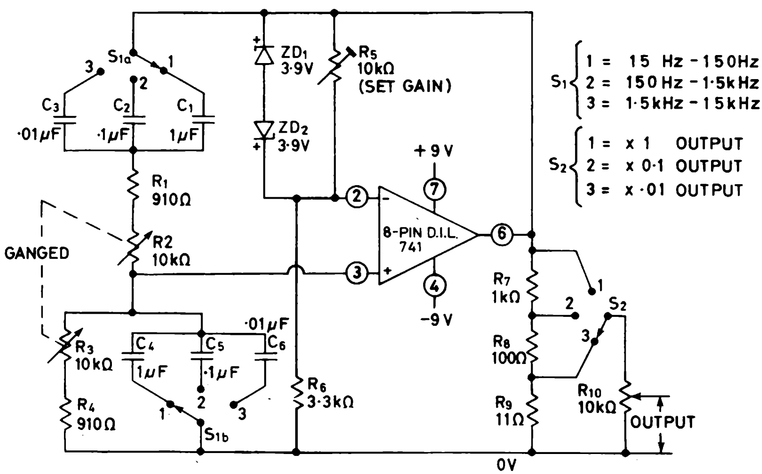


Fig. 1.9. Three-decade (15 Hz to 15 kHz) Wien-bridge oscillator

Finally, *Figure 1.9* shows the circuit of a useful variable-frequency Wien oscillator that covers the range 15 Hz to 15 kHz in three switched decade ranges. The circuit uses zener-diode amplitude regulation, and its output is adjustable by both switched and fully-variable attenuators.

L–C oscillator circuits

C–R sine wave oscillators are useful for generating signals ranging from a few hertz up to several tens or hundreds of kilohertz. L–C oscillators, on the other hand, are useful for generating signals from a few tens of kilohertz up to hundreds of megahertz. *Figure 1.10* shows the basic

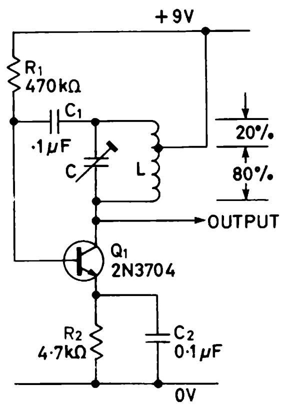


Fig. 1.10. Basic Hartley oscillator

circuit of one of the most fundamental of all L–C oscillators, the so-called Hartley circuit. Most other L–C oscillator circuits, such as the Colpitts and the Clapp or Gouriet types, are derived from this basic circuit.

The operating theory of the *Figure 1.10* circuit is fairly simple. The collector current of transistor Q_1 flows to the positive supply rail via the lower section of coil L, which is typically tapped 20 per cent down from its top. Because of this tapping, the coil gives an auto-transformer action, and the voltage signal appearing at the top of the coil is 180° out of phase with the voltage signal appearing at its low (Q_1 collector) end. The voltage signal appearing at the top of the coil is coupled to the base (input) of the transistor via isolating capacitor C_1.

Tuning capacitor C is wired across coil L to form a tuned circuit. A feature of any $L-C$ tuned circuit is that the phase relationship between its energising current and induced voltage varies over the range $-90°$ to $+90°$, and equals zero at a 'centre' frequency given by $f = 1/2\pi\sqrt{LC}$; see *Figure 8.4 and 8.5* design charts.

Thus, at this 'centre' frequency and no other, the phasing action of the tuned circuit causes the collector current and voltage of Q_1 to be in phase, so that a 180° phase shift occurs between the base and collector voltage signals of the transistor, precisely complementing the phase shift that occurs between the top and bottom of the tuned circuit. The circuit thus automatically oscillates at this centre frequency, so long as the transistor has enough gain to counter the losses of the tuned circuit. This 'gain' requirement is very easily met.

It should be noted that the $L-C$ oscillator does not usually require any kind of automatic gain control in order to produce good sine waves. Usually the 'Q' of the tuned circuit is sufficient to reduce harmonic signals to negligible values, thus giving good waveform purity, even when the actual transistor stage gain is grossly excessive to requirements.

Note from the above descriptive paragraphs that the $L-C$ oscillator circuit action is dependent on some kind of 'common signal' tapping point being made into the tuned circuit, so that an autotransformer action can be obtained from it. This tapping point does not have to be

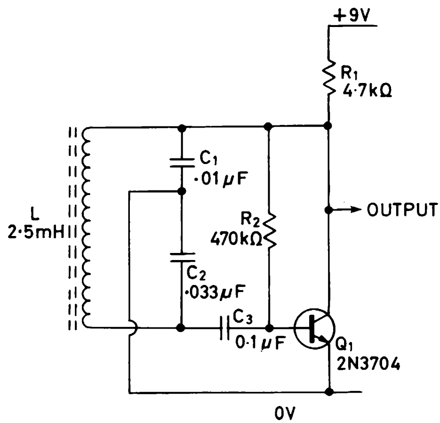


Fig. 1.11. 37 kHz Colpitts oscillator

made in the actual tuning coil, and can be made into the tuning capacitor if preferred, as in the Colpitts oscillator shown in *Figure 1.11*. With the component values shown, this particular circuit oscillates at a frequency of about 37 kHz.

Note in the Colpitts oscillator circuit that C_1 is in parallel with the output capacitance of transistor Q_1, and C_2 is in parallel with the input capacitance of Q_1. Consequently, changes in Q_1 capacitance (due to thermal shifts, etc.) cause a change in frequency. This effect can be minimised (and good frequency stability obtained) by making C_1 and C_2 large relative to the capacitances of Q_1.

A modification of the Colpitts oscillator, known as the Clapp or Gouriet oscillator, is shown in *Figure 1.12*. Here, a further capacitor

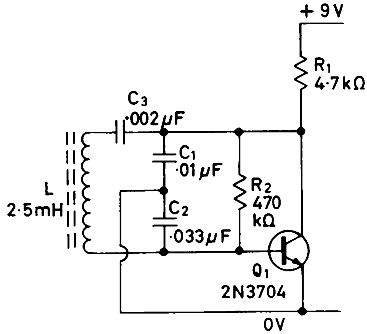


Fig. 1.12. 80 kHz Clapp or Gouriet oscillator

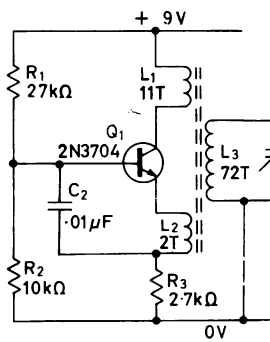


Fig. 1.13. Basic Reinartz oscillator

(C_3) is connected in series with L of the tuned circuit, and has a value that is small relative to C_1 and C_2. Consequently, the resonant frequency of the circuit is determined mainly by the values of L and C_3, and is substantially independent of variations in the transistor capacitances. This circuit thus gives excellent frequency stability. With the component values shown, this circuit oscillates at approximately 80 kHz.

It should be noted that the operating frequency formulae for the *Figure 1.11 and 1.12* circuits are the same as that of the *Figure 1.10* circuit, but that in *Figure 1.11* the effective value of the tuning '*C*' is equal to the series combination of C_1 and C_2, and in *Figure 1.12* is equal to the series combination of C_1-C_2 and C_3.

Finally, *Figure 1.13* shows the basic circuit of the so-called Reinartz oscillator. Here, the tuning coil has three inductively-coupled windings. Positive feedback is obtained in the circuit by coupling the collector and emitter signals of the transistor via windings L_1 and L_2. Both these inductors are also coupled to L_3, and the circuit oscillates at a frequency that is essentially determined by L_3 and C_1. The diagram shows typical coil-turns ratios for a circuit designed to oscillate at a few hundred kilohertz.

I.C. sine-wave generator circuits

A number of companies produce special-purpose waveform-generator integrated circuits capable of producing good sine waves in the low- to medium-frequency range. These i.c.s produce the sine waves in synthesised form. They contain a *C–R* oscillator that generates a linear triangle waveform, and this basic triangle is then shaped into sine form via either a diode matrix or a non-linear amplifier. One of the most useful of these waveform-generator i.c.s is the XR-2206, manufactured by Exar Integrated Systems Inc. of America.

The operating details of the XR-2206 i.c. are briefly described in Appendix 1. For the present, however, it is sufficient to know that the device can readily be made to generate good sine waves at frequencies ranging from a fraction of a hertz to a few hundred kilohertz, that the frequency is determined by *C–R* components, that the generated sine-wave distortion can readily be reduced to a typical value of 0.5 per cent, and that the i.c. can be powered from a single supply in the range 10 V to 26 V or from split supplies in the range ±5 V to ±13 V.

Figure 1.14 shows how the XR-2206 can be used as a simple variable-frequency sine-wave generator that uses a single power supply. The operating frequency of the circuit is inversely proportional to the values of C_1 and R_1-R_2, and can be varied over the range 10 Hz to 100 kHz in four decade ranges by using the C_1 values shown. The amplitude of the generated output signal is fully variable via R_5. The sine-wave distortion of this basic circuit is typically less than 2.5 per cent.

Figure 1.15 shows how the above circuit can be modified for split power-supply operation, and how the sine-wave distortion can be reduced to a typical value of 0.5 per cent by adjustment of preset

controls R_4 and R_5. These two controls are simply adjusted in unison to give the best possible waveform when the circuit is first constructed, and require no further adjustment thereafter.

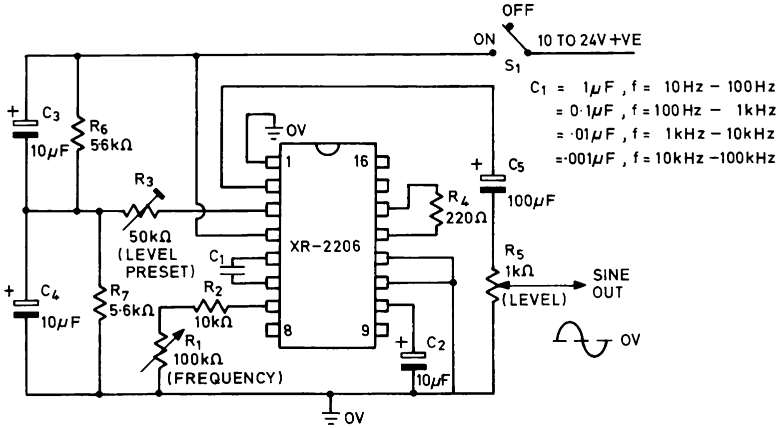


Fig. 1.14. Simple single-supply i.c. sine-wave generator

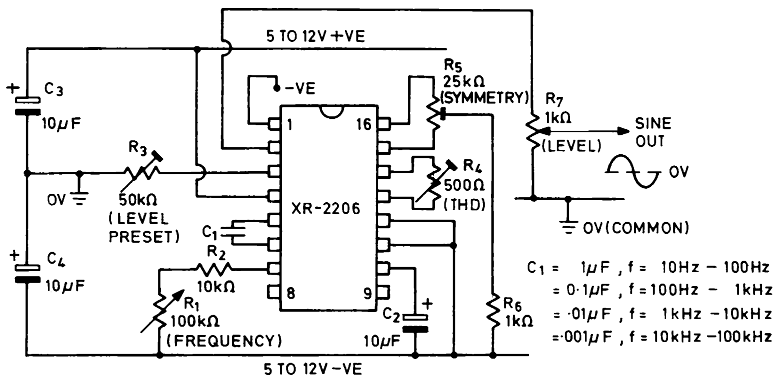


Fig. 1.15. High-quality split-supply i.c. sine-wave generator

Note in the *Figure 1.14 and 1.15* circuits that the maximum output signal can be preset via R_3. This control should always be adjusted to give a maximum output that is less than 2 V r.m.s., otherwise excessive sine-wave distortion may result.

CHAPTER 2

SQUARE AND PULSE GENERATORS

Square and pulse waveforms are probably the easiest of all waveforms to produce, particularly at low to medium frequencies. These waveforms can be generated by 'conversion' from existing waveforms, or can be produced directly from a wide variety of solid-state generator circuits. Thirty practical square and pulse generator circuits are described in this chapter.

Sine-to-square converter circuits

Existing symmetrical waveforms, such as sine waves, can readily be converted into square waves by feeding them through a Schmitt trigger circuit. *Figure 2.1* shows a practical transistor Schmitt trigger circuit that can be used for this purpose. This circuit needs an input drive signal of 0.5 V r.m.s. or greater. The square-wave output signal symmetry varies with the amplitude of the sine wave input signal, so R_1 must be adjusted to give the best output symmetry. The circuit acts as a good sine-to-square converter up to frequencies of a few hundred kilohertz, and the square-wave output rise time is only a fraction of a microsecond when the output is lightly loaded.

A COS/MOS i.c. version of the Schmitt sine/square converter circuit is shown in *Figure 2.2*. The i.c. used here is a type CD4093 quad 2-input NAND Schmitt trigger. In the application shown, only one of the four available gates of the i.c. is used, the remaining three being disabled by tying their input terminals to the zero volts rail.

The *Figure 2.2* circuit gives an excellent square-wave output, with typical rise and fall times less than 100 ns when the output is loaded by 50 pF. The input triggering sensitivity of the circuit depends on the

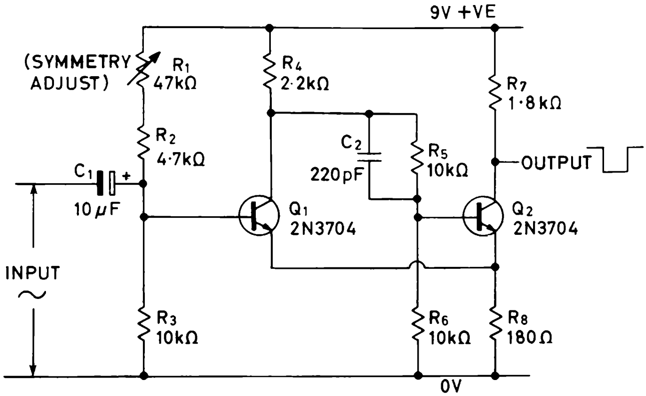


Fig. 2.1. Schmitt sine/square converter

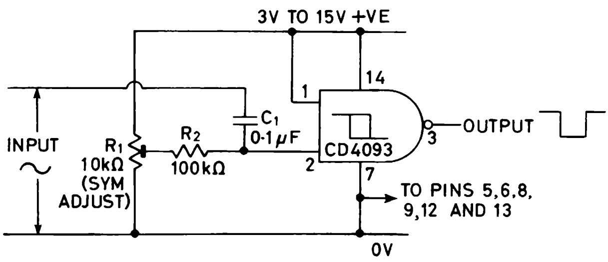


Fig. 2.2. COS/MOS sine/square converter

supply-line voltage used, and typically equals 0.6 V peak-to-peak with a 5 V supply, and 1.7 V peak-to-peak with a 10 V supply. The circuit has an input impedance of 100 kΩ. Preset control R_1 should be adjusted to give the best possible waveform symmetry.

Transistor astable multivibrator circuits

Repetitive square and rectangular waves can be generated directly in a variety of ways. One easy way is to use the basic transistor astable multivibrator circuit shown in *Figure 2.3*. This circuit is a self-oscillating

regenerative switch, in which the on and off periods of the circuit are controlled by the $C_1 - R_1$ and $C_2 - R_2$ time constants. If these time constants are equal ($C_1 = C_2$ and $R_1 = R_2$), the circuit acts as a square-wave generator, and operates at a frequency of approximately $1/1.4C_1R_1$; see *Figure 8.6* design chart. Thus the frequency can be decreased by raising the values of $C_1 - C_2$ or $R_1 - R_2$, or vice versa. The frequency

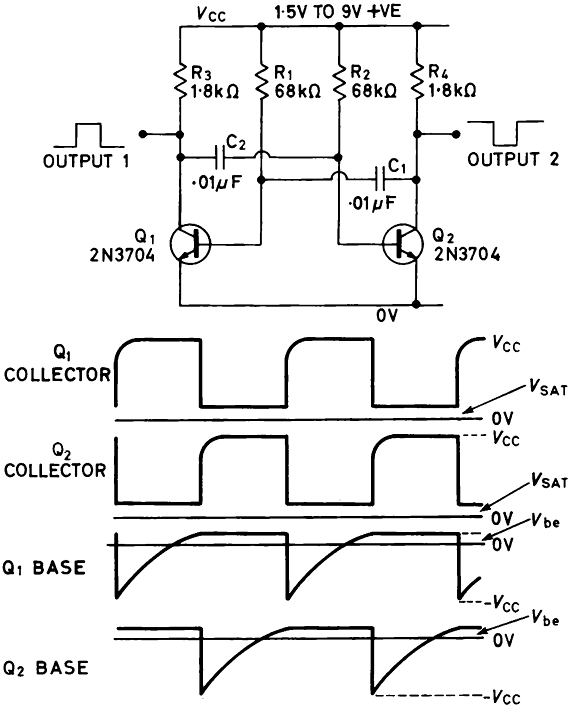


Fig. 2.3. Circuit and waveforms of basic 1 kHz transistor astable multivibrator

can be made variable by using twin-gang variable resistors (in series with 10 kΩ limiting resistors) in place of R_1 and R_2. The operating frequency of the circuit can be synchronised to that of an external signal of higher frequency by coupling part of the external signal into the timing networks of the astable circuit.

Outputs can be taken from either collector of the *Figure 2.3* circuit, and the two outputs are in anti-phase. The operating frequency of the circuit is substantially independent of supply-rail values in the range 1.5 V to 9 V. The upper supply-voltage limit is set by the fact that, as

the transistors switch regeneratively at the end of each half-cycle, the base–emitter junction of one transistor is reverse-biased by an amount roughly equal to the supply voltage. Consequently, if the supply voltage exceeds the reverse base–emitter breakdown voltage of the transistor, the timing operation of the circuit will be upset. This snag can be overcome by using the circuit modifications shown in *Figure 2.4*.

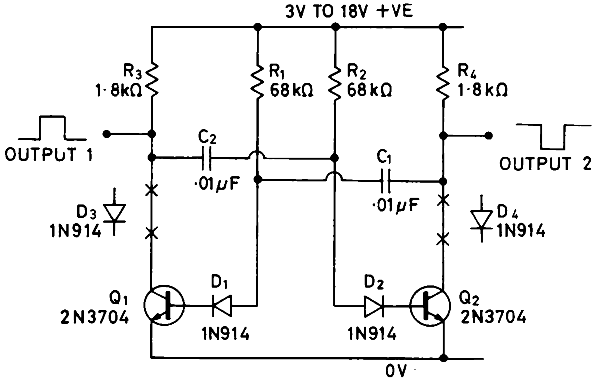


Fig. 2.4. Frequency-corrected 1 kHz transistor astable multivibrator

Here, a silicon diode is wired in series with the base input terminal of each transistor, and effectively raises the reverse base–emitter breakdown voltage of each transistor to a value greater than the reverse breakdown voltage of the diode. The protected *Figure 2.4* circuit can be used with any supply voltage in the range 3 V to 18 V, and gives a frequency variation of only 2 per cent when the supply voltage is varied from 6 V to 18 V.

Frequency stability can be further enhanced, if necessary, by wiring diodes in series with the collector of each transistor, as also shown in the diagram. In this case the frequency variation may typically be only 0.5 per cent when the supply voltage is varied from 6 V to 18 V. The object of using these two additional diodes is to make the effective (transistor plus diode) output saturation voltages of the transistors equal to the effective (transistor plus protection diode) input 'on' voltage of the transistors. In the ideal case, if these two voltages are precisely equal, the circuit will exhibit zero frequency change when the supply voltage is varied over the range 6 V to 18 V.

The leading edges of the two astable circuits of *Figures 2.3 and 2.4* are slightly rounded. The lower the values of R_1 and R_2 become, relative to collector resistors R_3 and R_4, the worse this waveform

rounding becomes. Conversely, the larger the values of R_1 and R_2 relative to R_3 and R_4, the better the waveshape will be. The maximum permissible values of R_1 and R_2 are determined by the current gains of the transistors, and equal $h_{FE} \times R_3$ (or R_4). Taking a minimum h_{FE} of 90 for the 2N3704 transistor, this means that the maximum permissible values of R_1 and R_2 are 162 kΩ in these two circuits.

Some of the limitations of the *Figure 2.3 and 2.4* circuits can be overcome by using Darlington or super-alpha connected transistors in place of Q_1 and Q_2, as shown in the *Figure 2.5* long-period astable

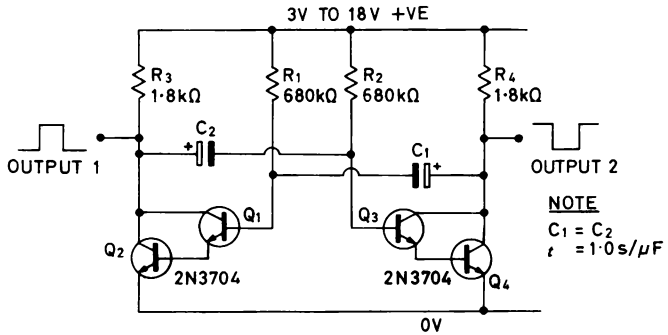


Fig. 2.5. Long-period transistor astable multivibrator

multivibrator circuit. Here, R_1 and R_2 can be given any value in the range 10 kΩ to 12 MΩ, and the circuit can be used with any supply voltages in the range 3 V to 18 V. With the resistance values shown, this circuit gives a total period or cycle time of about one second per microfarad when C_1 and C_2 have equal values.

The rounding of the leading edges of the *Figure 2.3 and 2.4* waveform-generator circuits occurs because the collector voltage of each transistor is prevented from rising immediately to the positive-rail voltage as the transistor turns off, because of loading by its cross-coupled timing capacitor. This deficiency can be overcome, and excellent square waves obtained, by effectively disconnecting the capacitor from the collector of its transistor as it turns off, as in the 1 kHz generator of *Figure 2.6*. Here, D_1 and D_2 are used to disconnect the timing capacitors at the moment of regenerative switching. The main time constants of the circuit are again determined by C_1–R_1 and C_2–R_2. The effective collector loads of Q_1 and Q_2 are equal to the parallel resistances of R_3–R_4 and R_5–R_6 respectively.

Operation of the basic astable multivibrator relies on slight imbalances of the transistor characteristics, so that one transistor turns on slightly

faster than the other when power is first applied. If the voltage to the circuit is applied by slowly increasing it from zero volts, both transistors may turn on simultaneously, in which case oscillation will not be

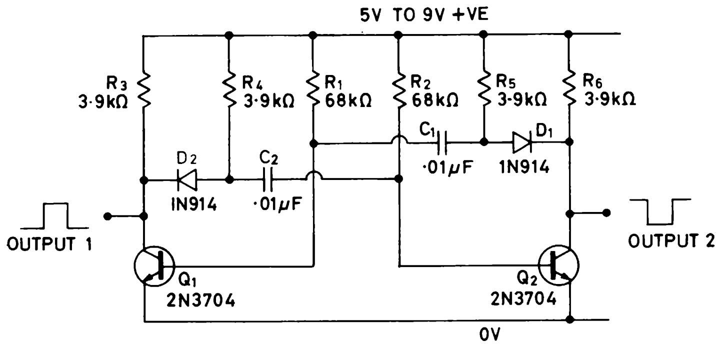


Fig. 2.6. 1 kHz astable with waveform correction

obtained. This snag can be overcome by using the sure-start circuit of *Figure 2.7*, in which the timing resistors are connected to the transistor collectors in such a way that only one transistor can ever be turned on at a given moment.

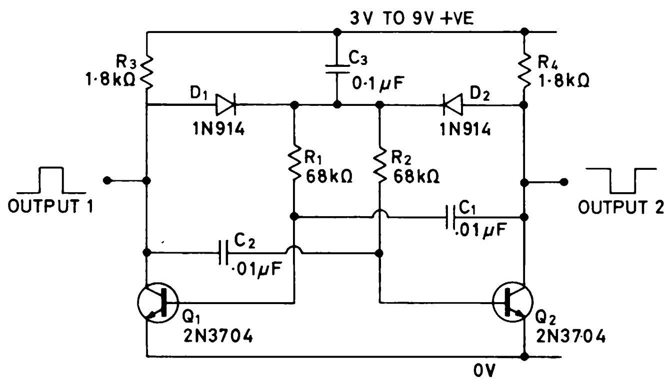


Fig. 2.7. 1 kHz astable with sure-start facility

The transistor astable circuits that we have looked at so far are designed to give a symmetrical output waveform, with a 1 : 1 mark/space ratio. A non-symmetrical waveform can be obtained by simply making one set of astable time-constant components larger than the other.

Figure 2.8a shows the connections for making a fixed-frequency (about 1100 Hz) variable mark/space ratio waveform generator, in which the ratio can be fully varied over the range 1 : 10 to 10 : 1.

The leading edges of the output waveforms of the above circuit may be objectionably rounded for some applications when the mark/space

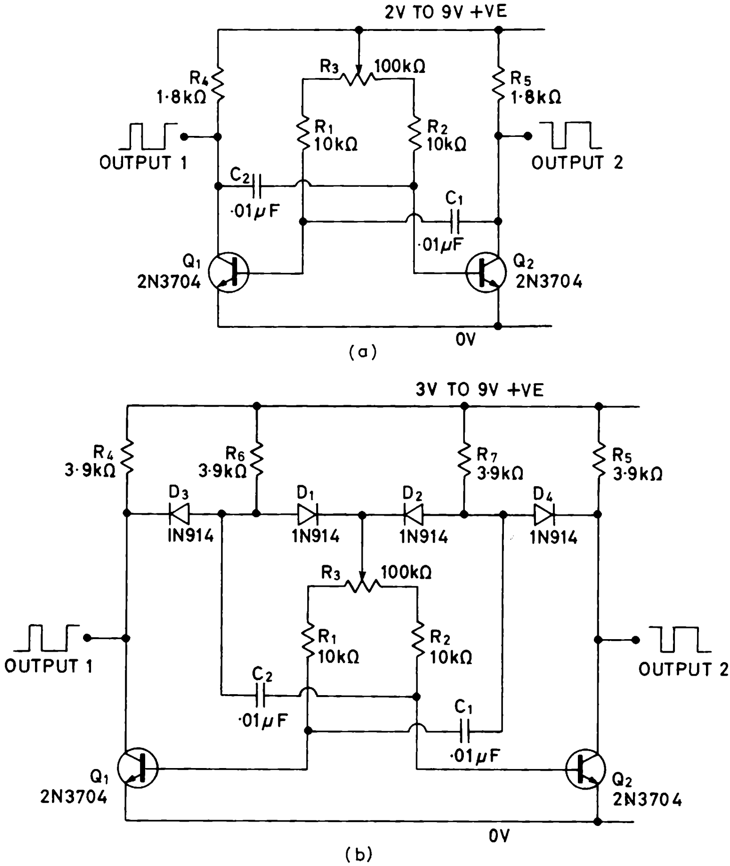


Fig. 2.8. Variable mark/space ratio astable multivibrator operating at approximately 1100 Hz; (a) basic version; (b) improved version with waveform-correction and sure-start facility

control is set at its extreme positions. Similarly, the circuit may be difficult to start if the supply voltage is applied to the circuit slowly. Both of these snags can be overcome by using the connections of *Figure 2.8b*, in which the circuit is fitted with sure-start and waveform-correction diodes.

Op-amp relaxation oscillator circuits

Good square waves can be generated by using an operational amplifier in the basic relaxation oscillator configuration shown in *Figure 2.9a*. This circuit requires the use of dual power supplies, and because of the slew-rate limitations of the op-amp its output waveform rise and fall times are generally not as good as those obtained from transistor astable multivibrator circuits. Great advantages of the op-amp circuit, however, are that it offers excellent frequency stability, and that its operating frequency can be varied over a wide range by altering any one of a number of component values.

Basically, the operation of the *Figure 2.9a* circuit is such that C_1 first charges up via R_1 until the C_1 voltage rises to a positive value determined by the R_2–R_3 ratio, at which point the op-amp switches regeneratively and C_1 starts to discharge via R_1 until the C_1 voltage falls to a negative value determined by the R_2–R_3 ratio, at which point the op-amp again switches regeneratively, and the whole sequence repeats itself. The action is such that a symmetrical square wave is developed at the output of the op-amp, and a non-linear triangle waveform is developed across C_1; each waveform swings either side of the zero-volts line.

Note that the operating frequency of the circuit can be varied by altering the R_1 or C_1 values, or by altering the R_2–R_3 ratios. *Figure 2.9b* shows the practical circuit of a simple 500 Hz to 5 kHz op-amp square-wave generator, in which frequency variation is obtained by altering the attenuation ratio of the R_2–R_3–R_4 potential divider.

Figure 2.9c shows how the above circuit can be improved by using R_5 to preset the range of the R_3 'frequency' control, and by using R_6 as an output amplitude control.

Figure 2.10 shows how the above circuit can be modified to make a general-purpose square-wave generator that covers the range 2 Hz to 20 kHz in four switched decade ranges. Note that preset controls R_1, R_3, R_5 and R_7 are used to precisely set the minimum frequencies of the 2 Hz–20 Hz, 20 Hz–200 Hz, 200 Hz–2 kHz, and 2 kHz–20 kHz ranges respectively.

Finally, *Figure 2.11* shows how the basic relaxation oscillator circuit can be modified so that it provides both a variable frequency and a variable mark/space ratio output. The M/S ratio is variable via R_1, and the circuit action is such that C_1 charges up via R_2–D_1 and the left-hand side of R_1, and discharges via R_2–D_2 and the right-hand side of R_1. The M/S ratio is variable over the range 11 : 1 to 1 : 11, and the frequency is variable over the range 650 Hz to 6.5 kHz.

It should be noted that each of the *Figure 2.9 to 2.11* circuits can be built around either a 741 or a 709 operational amplifier, but that the 709 op-amp gives the better output waveform because of its higher slew rate.

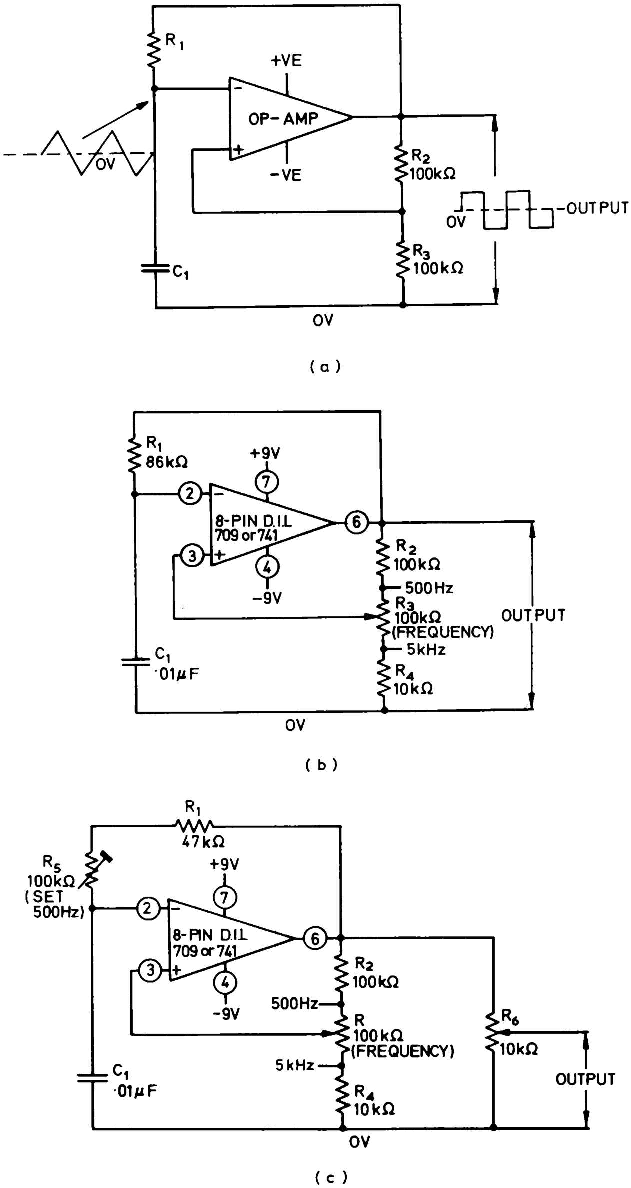


Fig. 2.9. (a) Basic op-amp relaxation oscillator circuit; (b) simple 500 Hz to 5 kHz square-wave generator; (c) improved version of (b)

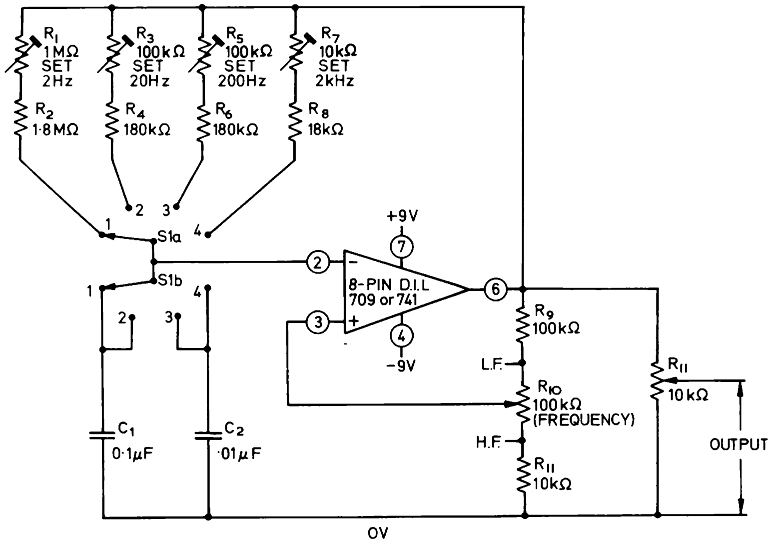


Fig. 2.10. Four-decade (2 Hz to 20 kHz) square-wave generator

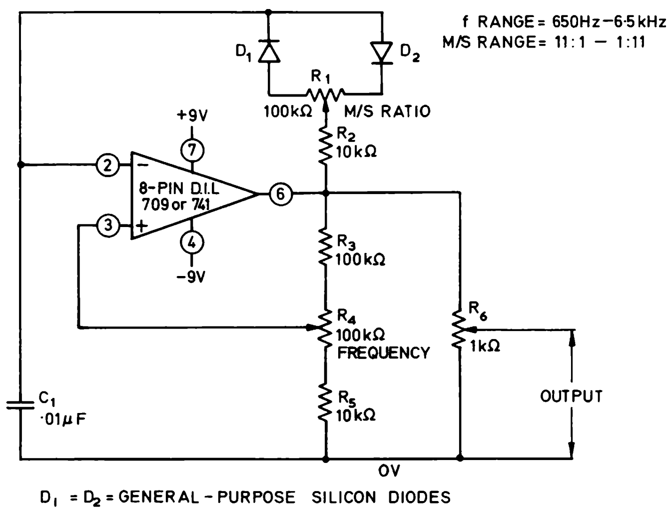


Fig. 2.11. Variable-frequency, variable mark/space ratio square-wave generator

COS/MOS astable circuits

Some digital integrated circuits can be used to make excellent square-wave generators. A very useful and inexpensive device in this respect is the CD4001 quad 2-input COS/MOS NOR gate, manufactured by RCA. *Figure 2.12a* shows how one half of a CD4001 can be used to

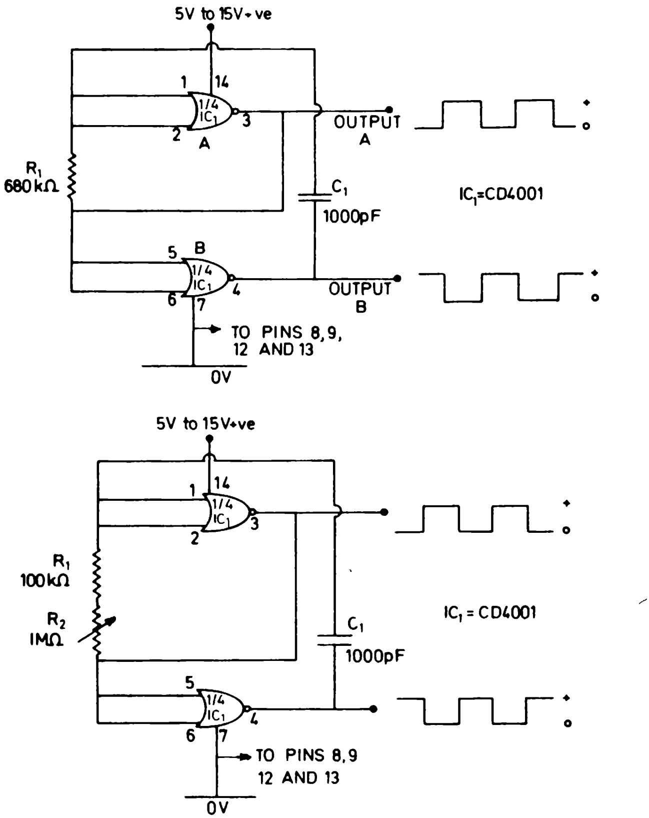


Fig. 2.12. COS/MOS astable multivibrator: (a) basic (1 kHz); (b) variable-frequency (600 Hz to 6 kHz)

make a basic 1 kHz astable multivibrator that can be used with any supply in the range 5 V to 15 V. Note that only two of the four available gates of the i.c. are used in this circuit, and that the two unused gates are disabled by strapping their input terminals to the zero-volts rail. Also note that the two gates that are used are connected as simple pulse inverters.

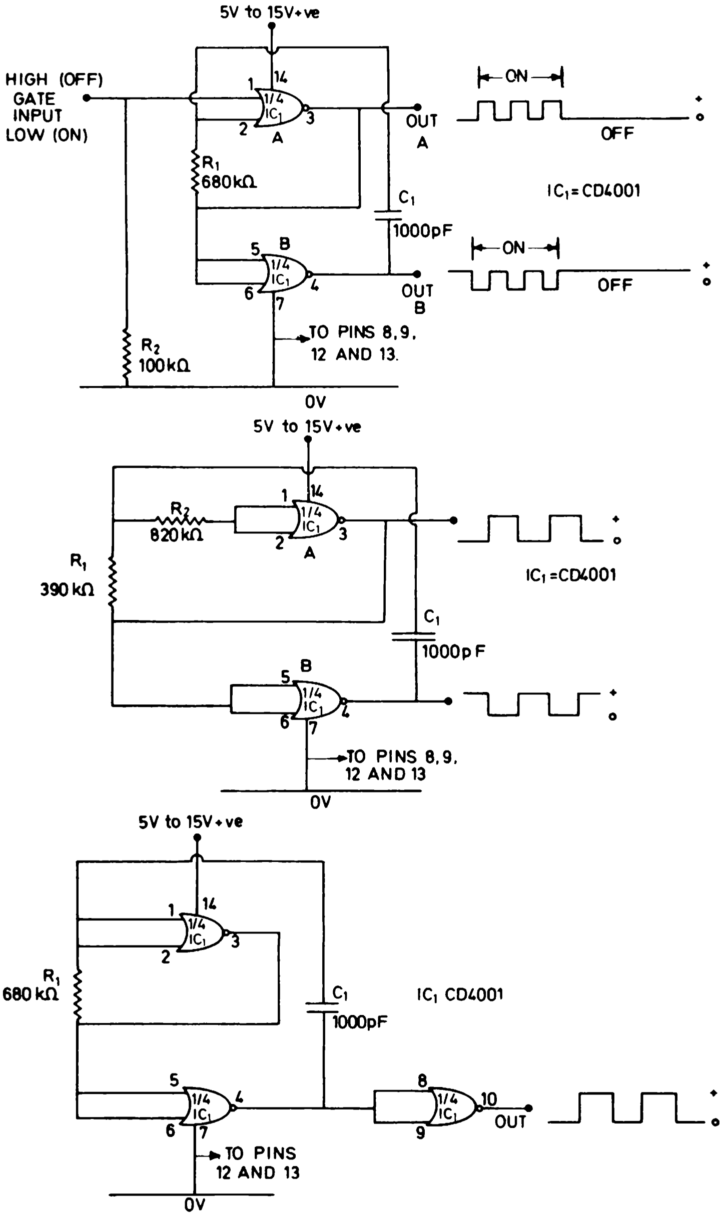


Fig. 2.13. 1 kHz astable multivibrator: (a) gated; (b) compensated; (c) buffered-output

Points to note about the basic COS/MOS astable circuit are that it uses only a single power supply, that it uses only two time-constant components (R_1 and C_1), that the value of time-constant component R_1 can be varied from less than 10 kΩ up to hundreds of megohms, and that the circuit generates a pair of anti-phase square-wave outputs. The only significant weakness of the basic circuit is that the symmetry of its square-wave output depends on the characteristics of the individual i.c. that is used, and a precisely symmetrical output is rarely obtained. Most times, the M/S ratio of the output will be within the range 5 : 4 to 4 : 5.

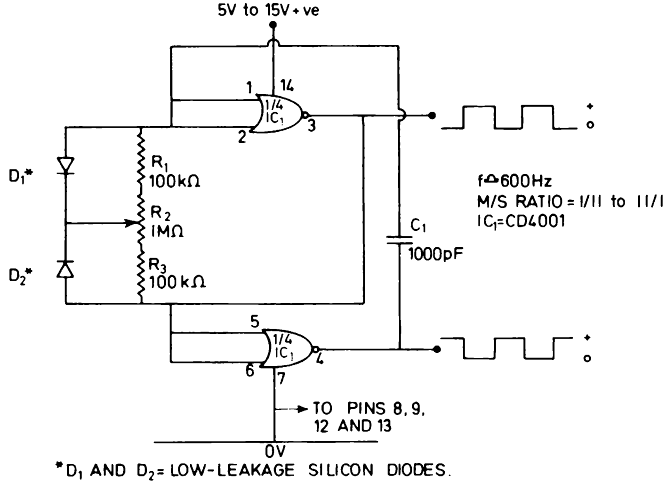


Fig. 2.14. Variable mark/space ratio astable multivibrator

The operating frequency of the basic COS/MOS astable circuit can be made variable by simply replacing fixed timing resistor R_1 with a fixed and a variable resistor in series, as shown in the practical circuit of *Figure 2.12b*. This particular circuit covers the frequency range 600 Hz to 6 kHz.

The basic COS/MOS astable circuit can be usefully modified in a number of ways. It can be converted into a gated astable multivibrator by using the connections shown in *Figure 2.13a.* Here, gate A is used as a NOR gate rather than as a simple inverter; the circuit can be gated 'on' by applying a low (zero or ground volts) signal to pin 1 of the i.c., and can be gated 'off' by applying a high (full positive-rail voltage) signal to pin 1 of the i.c.

Another circuit modification is shown in *Figure 2.13b*. Here, high-value resistor R_2 is simply wired in series with the input of gate A.

This resistor has the effect of reducing the influence of the individual i.c. characteristics on the final circuit performance, and so enhances the circuit's thermal stability and improves the symmetry of the output waveform.

Yet another modification is shown in *Figure 2.13c*. Here, one of the spare gates of the CD4001 i.c. is simply wired in series with the output of the astable circuit. This gate acts as an output buffer, and sharpens up the shape of the final output waveform and minimises the effects of varying output loads on the circuit's operating frequency.

Finally, *Figure 2.14* shows how the basic circuit can be modified so that it produces a variable mark/space ratio output. Here, the time constant of the circuit is determined by $C_1-D_1-R_3$ and the lower half of R_2 in one half-cycle, and by $C_1-D_2-R_1$ and the upper half of R_2 in the other half-cycle. The mark/space ratio of the circuit is variable over the range 1 : 11 to 11 : 1 via R_2, and the operating frequency of the circuit is approximately constant at 600 Hz at all settings of R_2.

Type 555 i.c. square-wave generator circuits

One i.c. that is exceptionally useful in square-wave generator applications is the device universally known as the '555 timer'. It is readily available in an 8-pin plastic dual-in-line package, and is produced by a number of manufacturers. The device can be powered by any supply in the range 4.5 V to 16 V. It has a low-impedance output that can source (supply) or sink (absorb) load currents up to 200 mA. When used in the astable mode its output produces typical rise and fall times of about 100 ns. It produces good square waves, with excellent stability, up to frequencies of about 100 kHz, and its frequency and M/S ratio can be accurately controlled with two external resistors and one capacitor.

Figure 2.15a shows the practical circuit of a basic 555 1 kHz astable multivibrator, together with the formulae that define the timing of the circuit. The circuit operation is such that C_1 first starts to charge exponentially via the series R_1-R_2 combination until eventually the C_1 voltage rises to $^2\!/_3\,V_{CC}$. At this point a regenerative switching action takes place, and C_1 starts to discharge exponentially via R_2 until eventually the C_1 voltage falls to $^1\!/_3\,V_{CC}$, at which point a second regenerative switching action takes place, and the whole sequence repeats itself.

Thus both the mark/space ratio and the frequency of the circuit are determined by the $R_1-R_2-C_1$ values. Note that if R_2 is very large relative to R_1, the operating frequency of the circuit is determined

mainly by the R_2 and C_1 values, and that a virtually symmetrical output waveform is generated. The graph of *Figure 2.15b* shows the approximate relationship between frequency and the C_1–R_2 values under the above condition.

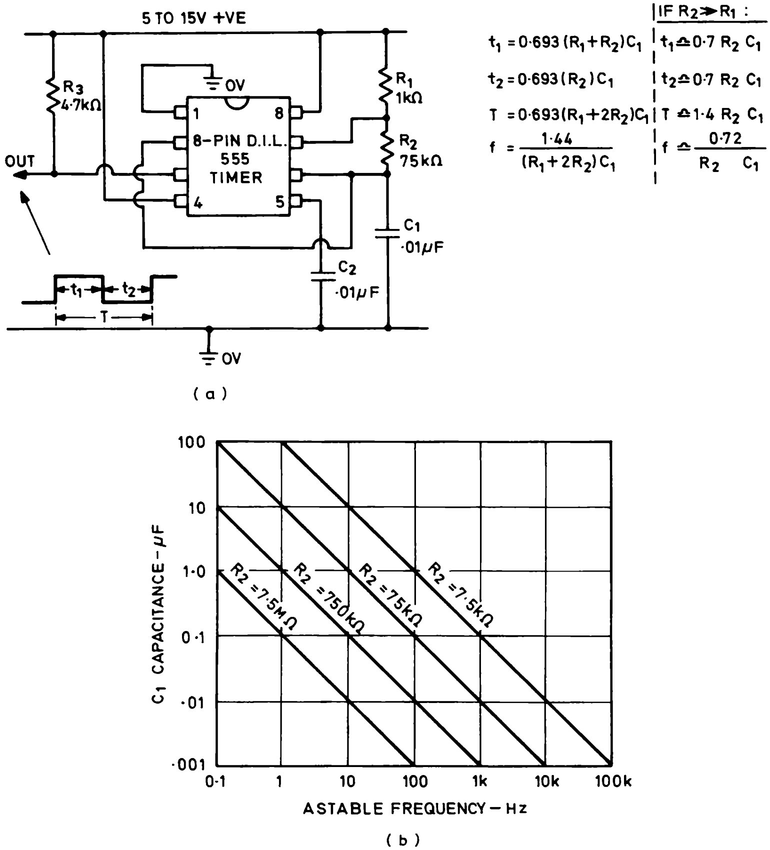


Fig. 2.15. (a) Basic circuit of 1 kHz astable multivibrator with timing formulae; (b) approximate relationship between C_1, R_2 and frequency when R_2 is large relative to R_1

In practice, the R_1 and R_2 values of the circuit can be varied from 1 kΩ up to tens of megohms.

The basic *Figure 2.15a* circuit can be usefully modified in a number of ways. *Figure 2.16*, for example, shows how it can be made into a variable-frequency square-wave generator by replacing R_2 with a fixed

and a variable resistor in series. With the component values shown, the frequency can be varied over the approximate range 650 Hz to 7.2 kHz via R_2.

Figure 2.17 shows how the circuit can be modified so that its 'mark' and 'space' periods are independently variable over the approximate

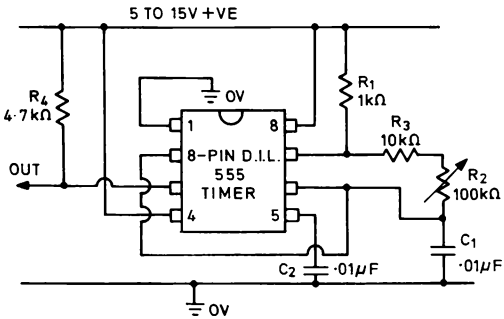


Fig. 2.16. Variable-frequency square-wave generator covers range 650 Hz to 7.2 kHz approximately

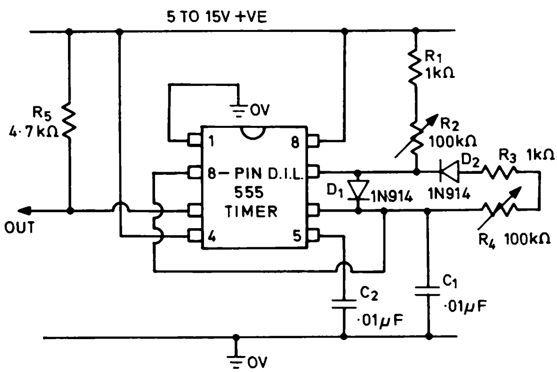


Fig. 2.17. Astable multivibrator with mark and space periods independently variable over approximate range 7.5 μs to 750 μs

range 7.5 μs to 750 μs. Here, timing capacitor C_1 alternately charges via R_1–R_2–D_1 and discharges via R_3–R_4–D_2.

Figure 2.18 shows how the circuit can be modified so that it acts as a fixed-frequency square-wave generator with a mark/space ratio or duty cycle that is fully variable from 1 per cent to 99 per cent. Here,

C_1 alternately charges via R_1 and the top half of R_2 and via D_1, and discharges via D_2–R_3 and the lower half of R_2. Note that the sum of the two timing periods is virtually constant, so the operating frequency is almost independent of the setting of R_2.

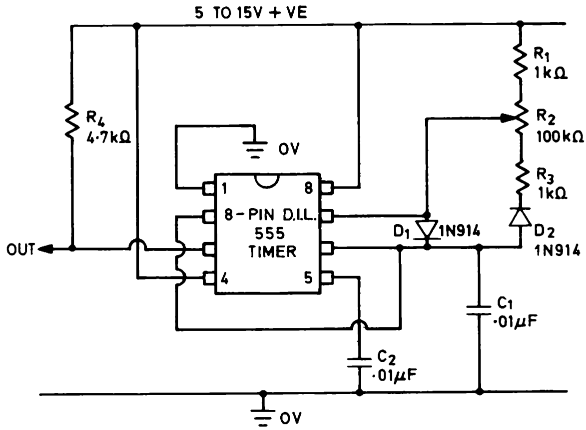


Fig. 2.18. Astable multivibrator with duty cycle variable from 1 to 99 per cent, frequency approximately constant at 1.2 kHz

The 555 astable circuit can be gated 'on' or 'off', via either a switch or an electronic signal, in a variety of ways. *Figures 2.19 and 2.20* show two basic ways of gating the i.c. via a switch.

The *Figure 2.19a and b* circuits are gated via the pin 4 (reset) terminal. The characteristics of this terminal are such that, if the terminal is biased significantly above a nominal value of 0.7 V, the astable is enabled, but if the terminal is biased below 0.7 V by a current greater than 0.1 mA (by taking the terminal to ground via a resistance less than 7 kΩ, for example) the astable is disabled and its output is grounded. Thus the *Figure 2.19a* circuit is normally on but can be turned off by closing S_1 and shorting pin 4 to ground, while the *Figure 2.19b* circuit is normally gated off via R_4 but can be turned on by closing S_1 and shorting pin 4 to the positive supply rail. These circuits can alternatively be gated by applying suitable electronic signals directly to pin 4 of the i.c.

The *Figure 2.20a and b* circuits are gated via the pin 2 (trigger) and pin 6 (threshold) terminals. The characteristic here is such that the circuit functions as a normal astable only as long as pin 6 is free to swing up to $^2/_3\,V_{CC}$ and pin 2 is not biased below $^1/_3\,V_{CC}$. If these pins are simultaneously driven below $^1/_3\,V_{CC}$, the astable action is immediately

terminated and the output is driven to the high state. Thus in *Figure 2.20a* the circuit is normally on but turns off when S_1 is closed. Note that an electronic signal can be used to gate the circuit by connecting

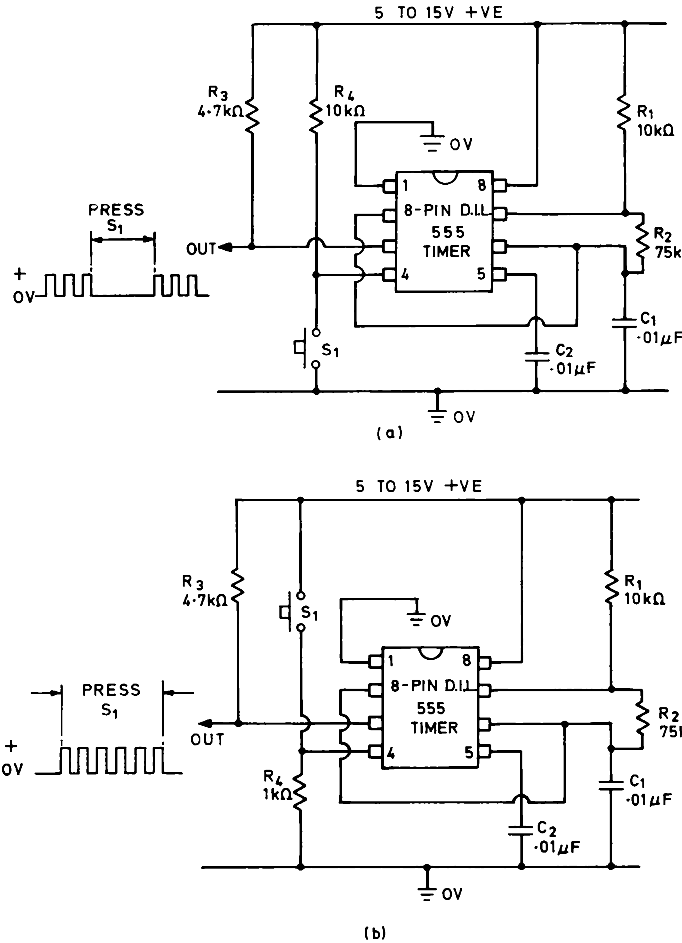


Fig. 2.19. Gated 1 kHz astable: (a) 'press-to-turn-off', (b) 'press-to-turn-on'

a diode as indicated and eliminating S_1. In this case the circuit will gate off when the input signal voltage is reduced below $1/3\,V_{cc}$.

The *Figure 2.20b* circuit is connected so that it is normally gated off by saturated transistor Q_1, but can be gated on by closing S_1 and thus

turning the transistor off. This circuit can be gated electronically by eliminating R_5 and S_1 and applying a gating signal to the base of Q_1 via a 10 kΩ limiting resistor. In this case the astable turns off when the input signal is high, and turns on when the input signal is reduced below 0.7 V or so.

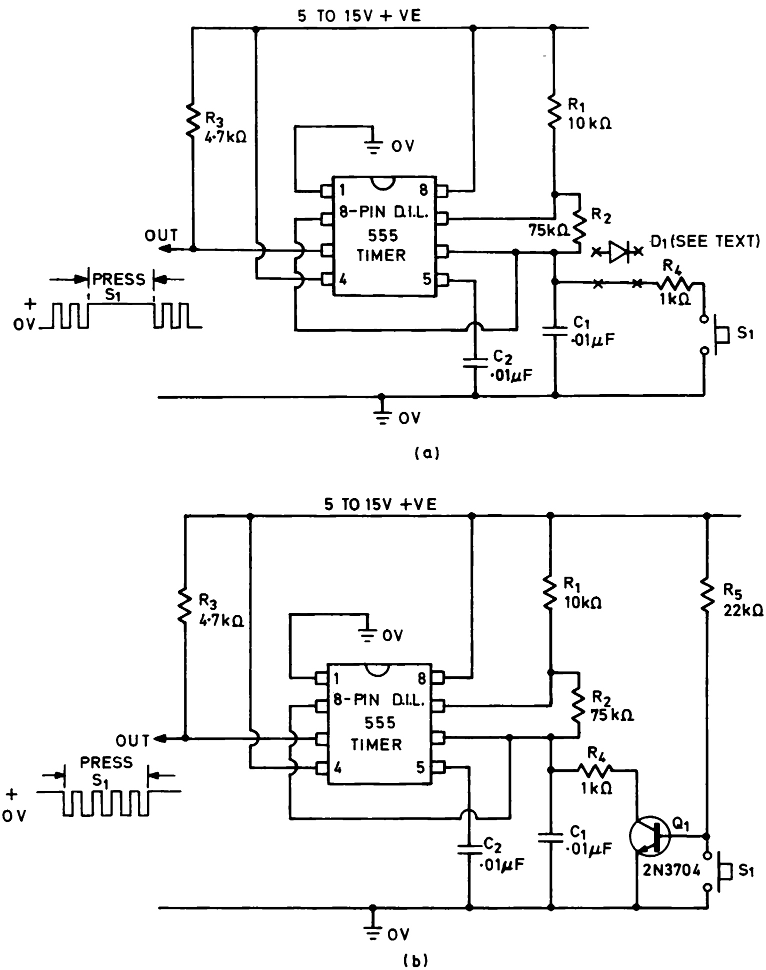


Fig. 2.20. Alternative gated 1 kHz astable: (a) 'press-to-turn-off', (b) 'press-to-turn-on'

Transistor monostable pulse-generator circuits

Pulse generators come in two basic types. They can be either self-triggering types, which inherently produce a continuous train of pulses, or they can be externally triggered types, which produce a single output on each application of an external trigger signal. Self-triggering pulse generators can be evolved from many of the so-called 'square-wave' generator circuits already described in this chapter: these circuits should simply be designed to give a non-symmetrical output, so that the 'on' period of the output waveform corresponds to the desired pulse width, and the reciprocal of the sum of the 'on' and 'off' times corresponds to the repetition frequency of the pulse.

Externally triggered pulse-generator circuits can be built using a variety of semiconductor technologies. The remainder of this chapter is devoted to such circuits, which, for the sake of simplicity, will from now on be referred to simply as 'triggered' pulse generators.

One of the most basic of all triggered pulse-generator circuits is the transistor monostable multivibrator. *Figure 2.21a* shows the practical circuit of a manually triggered generator of this type. In this circuit Q_1 is normally cut off, Q_2 is driven to saturation via R_1, and C_1 is fully charged. When S_1 is momentarily closed, a regenerative switching action is initiated in which Q_1 is driven to saturation and Q_2 is driven off by the resulting negative-going charge of C_1. As soon as this regenerative action is complete, C_1 starts to discharge via R_1, until eventually its charge falls to such a value that Q_2 starts to turn on again, at which point a second regenerative action is initiated in which the transistors revert to their original states and the action is complete. The basic waveforms of the circuit are shown in the diagram.

Thus a positive-going pulse is developed at the output of this circuit each time an input trigger signal is applied via S_1. The period (p) of the pulse is determined by the values of R_1 and C_1, and approximates $0.7 \times C_1 \times R_1$ (see the *Figure 8.7* design chart), where p is in microseconds, C is in microfarads and R is in kilohms. The period of the pulse of the *Figure 2.21a* circuit is substantially independent of variations in supply voltage over the range 3 V to 9 V, and approximates 50 ms per microfarad of C_1 value with the R_1 value shown.

Note in this basic circuit that the base–emitter junction of Q_2 is reverse-biased by a peak amount equal to the supply-voltage value during the operating cycle, and this factor limits the maximum supply voltage that can be used with a given transistor. Supply voltages greater than the reverse base–emitter breakdown value of Q_2 can be used in the circuit by simply wiring a silicon protection diode in series with the base of Q_2, as shown dotted in the diagram, to provide the same

'frequency correction' action as described for the transistor astable multivibrator circuit.

The value of timing resistor R_1 used in the basic monostable circuit must be large relative to R_5, but must be less than the product of R_6 and the h_{FE} of Q_2. Very long timing periods can be obtained by using

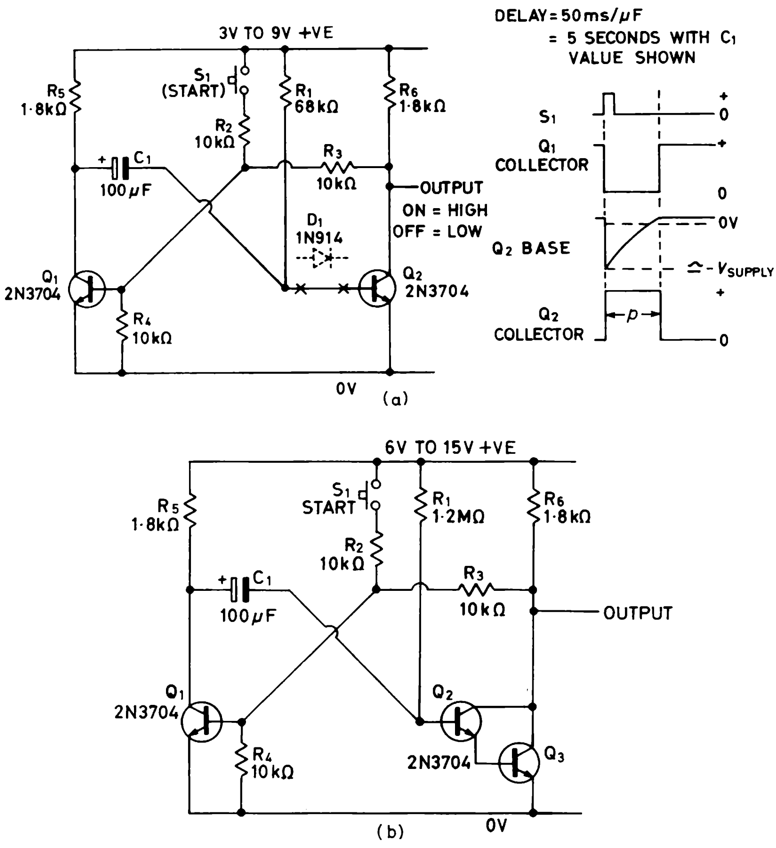


Fig. 2.21. Manually triggered transistor monostable pulse generator: (a) basic circuit and waveforms; (b) long-period (100 second) version

a Darlington or super-alpha pair of transistors in place of Q_2, thus giving a very high effective h_{FE} and enabling large values of R_1 to be used, as shown in the circuit of *Figure 2.21b*. This particular circuit can be used with any supply voltage in the range 6 V to 15 V, and gives a pulse output period of about 100 seconds with the R_1 and C_1 values shown.

A final point to note about the basic transistor monostable circuit concerns the input trigger signal. The circuit triggers on the application of a positive-going pulse to the base of Q_1. If this pulse is removed before the monostable completes its natural timing period, the period will end regeneratively in the manner already described. If, on the other hand,

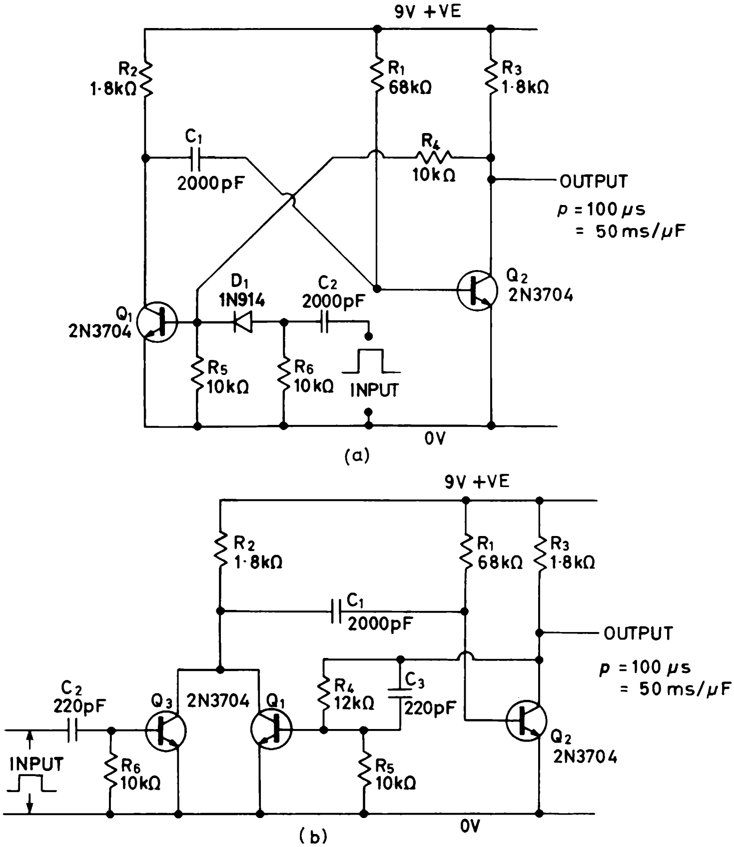


Fig. 2.22. Monostable multivibrator: (a) electronically triggered; (b) with gate input triggering

the trigger signal has not been removed by the time the monostable completes its natural timing period, the timing period will simply end non-regeneratively, and the output pulse will have a longer fall time and a longer period than in the former case.

The transistor monostable circuit can be triggered electronically in a variety of ways. *Figure 2.22a and b* shows two alternative ways of

obtaining electronic trigger action. In each case the circuit is triggered by a rectangular waveform with a short rise time, and this waveform signal is differentiated by the C_2–R_6 network to give a trigger pulse that has a duration that is short relative to the period of the desired output pulse. In the case of the *Figure 2.22a* circuit the differentiated input signal is discriminated by diode D_1 to give a brief positive trigger pulse to the base of Q_1 on each application of the external input signal. In the *Figure 2.22b* circuit the differentiated signal is fed to gate transistor Q_3, which enables the trigger signal to be quite independent of Q_1. Note in the latter circuit that 'speed up' capacitor C_3 is wired across feedback resistor R_4 to help improve the shape of the circuit's output pulse.

The *Figure 2.22a and b* circuits each give an output pulse period of about 100 μs with the component values shown. The period can be varied from a fraction of a microsecond to tens of seconds by suitable selection of the C_1 and R_1 time-constant values. The circuits can be triggered by sine or other non-rectangular waveforms by feeding these waveforms to the monostable circuits via a Schmitt trigger or similar sine/square converter circuit.

COS/MOS monostable pulse-generator circuits

The CD4001 quad 2-input NOR gate COS/MOS digital i.c. can be used as an excellent and very easily triggered monostable multivibrator.

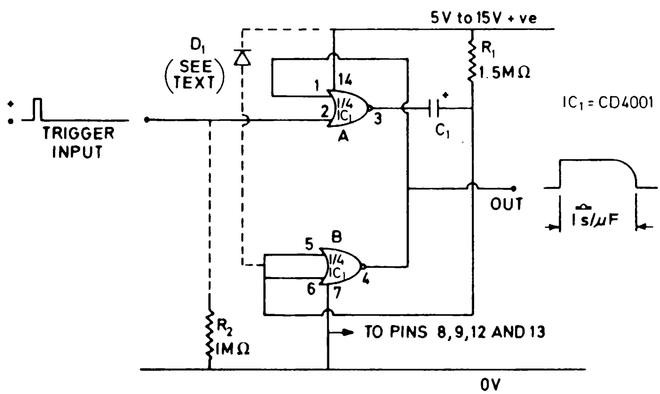


Fig. 2.23. Basic COS/MOS monostable multivibrator or pulse generator

Figure 2.23 shows the basic version of such a circuit. Here, gate A is used as a NOR logic element, and gate B is used as a simple pulse inverter. The circuit operates as follows.

Normally, when the circuit is in its quiescent state, the input to gate B is held high via R_1, so the output of gate B is low. Consequently both input terminals of gate A are low, and the output of gate A is high. Thus, since both ends of C_1 are high, C_1 is fully discharged.

Suppose now that a brief positive pulse is applied to the input of gate A. As soon as this trigger pulse is applied it drives the output of gate A to ground, and drags the input of gate B with it via discharged capacitor C_1. The output of gate B immediately goes high, and thus holds the output of gate A in the low state irrespective of the state of the original input trigger signal.

As soon as the output of gate A goes low as a result of the initial trigger action, C_1 starts to charge up via R_1, and an exponential rising voltage is applied to the input of gate B via the $R_1 - C_1$ junction. Eventually, after a delay determined by the R_1 and C_1 values, this voltage rises to the 'transfer' level of gate B; at this point the output of gate B switches back into the low state, and the output pulse is terminated.

If the trigger input terminal is in the low state at this point of time, the output pulse terminates regeneratively and C_1 discharges rapidly via the built-in protection diode of gate B (shown dotted as D_1 in the diagram) as the output of gate A switches back into the high state, thus completing the timing sequence. Alternatively, if the input trigger terminal is still in the high state at the moment that the output pulse terminates, the output pulse terminates non-regeneratively and C_1 continues to charge via R_1 because the output of gate A remains in the low state. C_1 eventually discharges rapidly via the input protection diode of gate B when the input trigger terminal of gate A finally goes to the low state. In either case, the duration of the output pulse is almost independent of the state of the input trigger terminal at the moment of pulse termination.

Note from the above description of circuit operation that the actual time period obtained from the circuit depends on the transfer voltage value of the individual CD4001 i.c. that is used in the circuit, as well as on the R_1 and C_1 values. In practice the transfer voltage value of this i.c. has a production spread of 30–70 per cent of supply voltage, so the actual timing period obtained from a given set of R_1 and C_1 values can vary considerably from one i.c. to another. The transfer-voltage value of any individual CD 4001 i.c. is not generally influenced by temperature variations, however, so the basic COS/MOS monostable circuit of *Figure 2.23* has good thermal stability. This particular circuit gives a period of roughly one second per microfarad of C_1 value when R_1 has a value of 1.5 MΩ. C_1 can have any value from a few picofarads to hundreds of microfarads, and R_1 can have any value from a few thousand ohms to thousands of megohms.

A point of particular importance to note about the basic COS/MOS monostable circuit of *Figure 2.23* is that it is actually triggered at the moment that the positive-going input trigger signal passes through the transfer voltage area of gate A, and the duration of the output pulse is almost independent of the subsequent state of the trigger terminal. Consequently, the circuit can be triggered by any shape of input waveform, irrespective of its rise time or duration. The circuit thus has outstandingly useful trigger characteristics.

The simple circuit of *Figure 2.23* suffers from a few minor snags, but is quite suitable for use in a number of simple practical applications. *Figure 2.24* shows how it can be used as a manually triggered pulse-generator or 'auto-turn-off time delay' circuit. The trigger pulse is

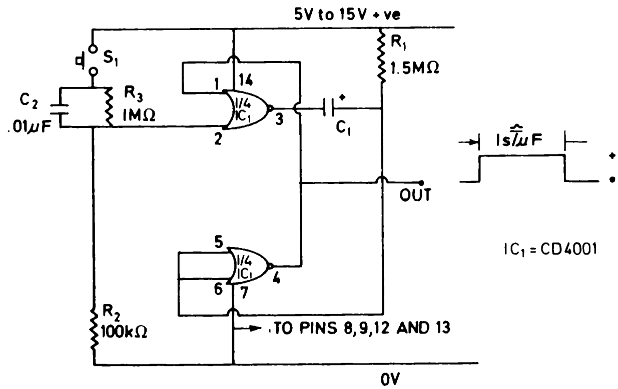


Fig. 2.24. Manually triggered COS/MOS monostable pulse generator

applied from the positive supply line via S_1 and C_2; R_3 is used to discharge C_2 when S_1 is released. The circuit gives an output pulse period of about one second per microfarad of C_1 value.

One of the minor snags of the basic *Figure 2.23* circuit is that it has a relatively long recovery time, since C_1 discharges via the comparatively 'imperfect' built-in protection diode of gate B at the end of each pulse-generating cycle. In practice, this means that the pulse length varies slightly with input frequency if the repetition period of the trigger signal is less than ten times that of the output pulse. This problem can be overcome by wiring a general-purpose germanium signal diode between the positive supply line and the input terminal of gate B, as shown in *Figure 2.25*. This modification enables stable pulses to be developed even at repetition periods that are only fractionally longer than the output pulse period.

The *Figure 2.25* circuit also shows how a complementary or anti-phase output can be obtained from the circuit by wiring one of the spare gates of the CD4001 as an inverter and connecting it between the output of the monostable and a separate output terminal.

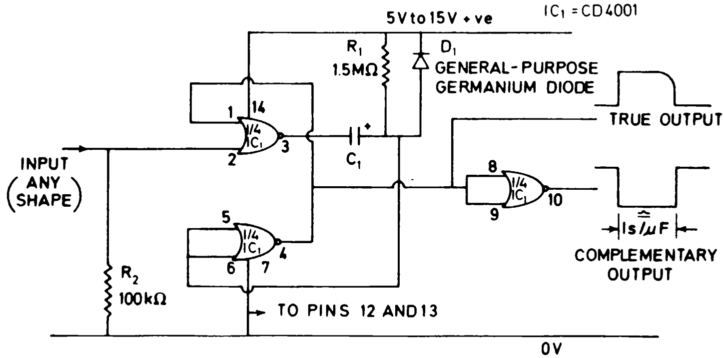


Fig. 2.25. Improved COS/MOS monostable with fast recovery and complementary output

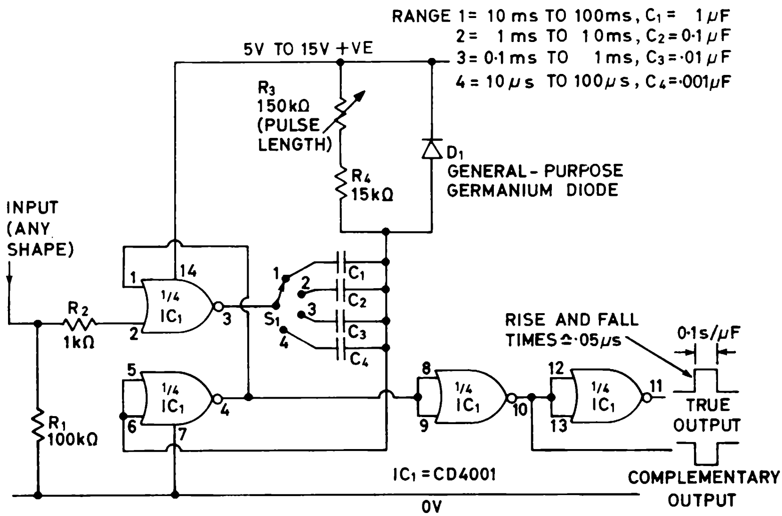


Fig. 2.26. Amateur's low-cost, wide-range (10 μs to 100 ms) COS/MOS pulse generator with true and complementary outputs

A second minor snag of the *Figure 2.23* circuit is that the trailing edge of its output pulse is slightly rounded. This can be overcome by wiring the two unused gates of the CD4001 as a non-inverting pulse amplifier connected between the output terminals of the monostable

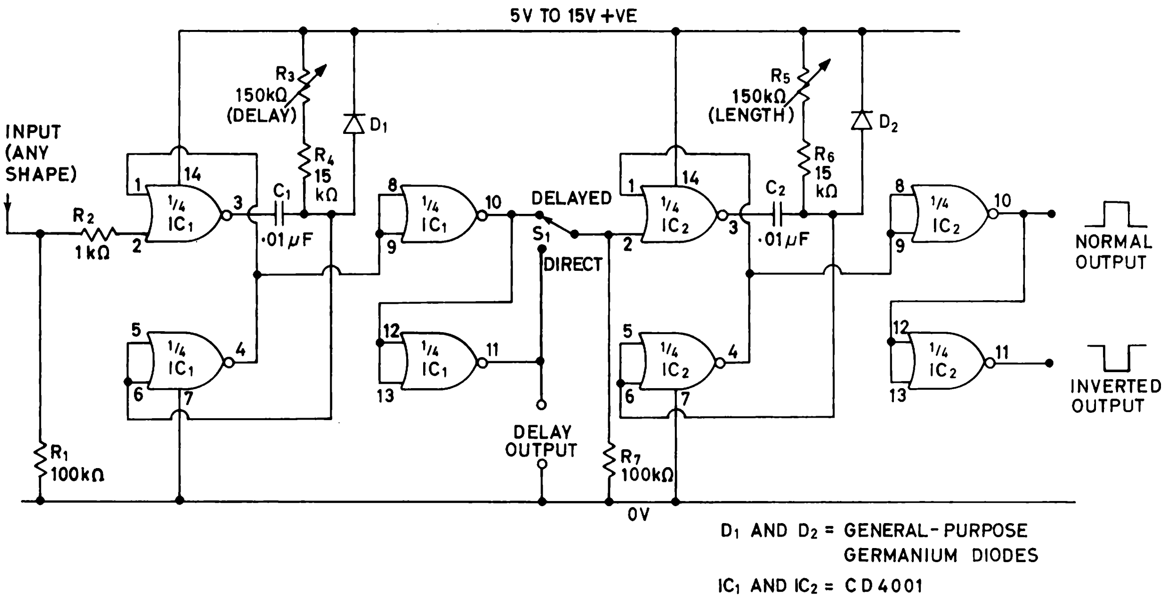


Fig. 2.27. Amateur's low-cost, delayed-pulse generator covering the range 0.1 ms to 1 ms

and the final output terminals of the circuit, as shown in *Figure 2.26*. This diagram also shows how the circuit can be used as a wide-range variable pulse generator, covering the range 10 μs to 100 ms in four switched decade ranges. The circuit incorporates the fast-recovery modification, and gives true complementary outputs. The pulses at the 'true output' terminals of the circuit have typical rise and fall times of about 0.05 μs.

The *Figure 2.26* circuit is suitable for use as an amateur's simple low-cost pulse generator; this can be used in conjunction with an existing sine- or square-wave generator, which provides the required trigger waveforms. Alternatively, a variable-frequency COS/MOS astable multivibrator can be built into the circuit and used as a built-in trigger generator.

Two of the simple *Figure 2.26* circuits can readily be interconnected to make an amateur's low-cost delayed-pulse generator, with independently controlled delay and pulse lengths. *Figure 2.27* shows the connections for making a single-range version of such a circuit. A multi-range version can be made by adding suitable range switching. Here, with S_1 in the 'delayed' position, the monostable formed by IC_1 is fired by the trigger input signal, and then, as the first monostable turns off, it

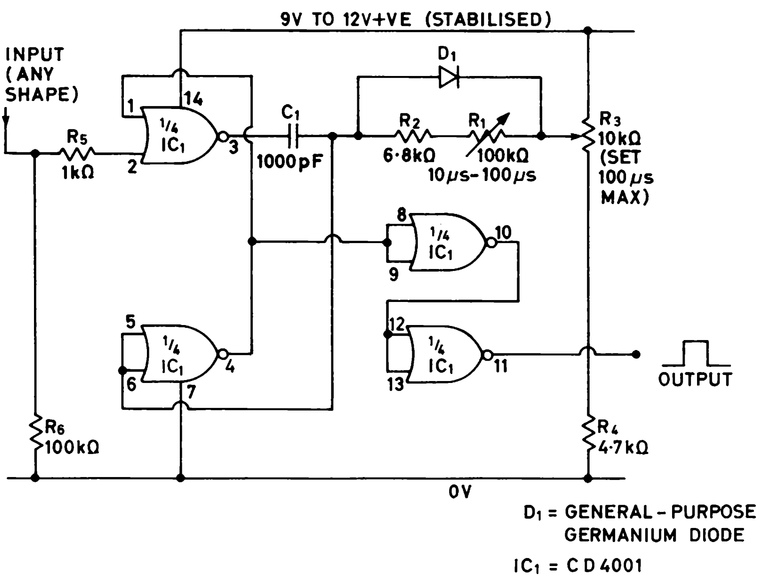
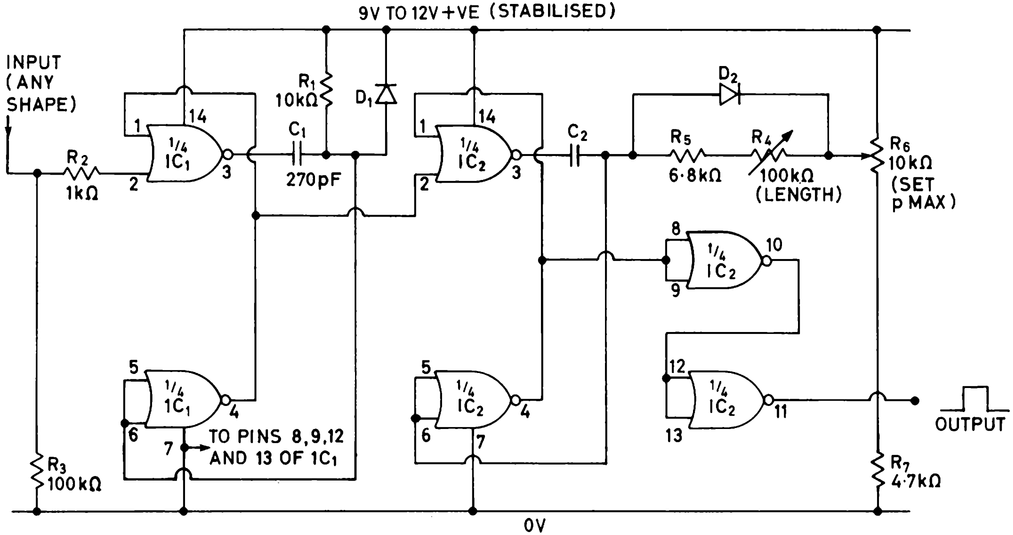


Fig. 2.28. 'Compensatable' monostable multivibrator covering the range 10 μs to 100 μs; performance can be made independent of CD4001 characteristics



D1 AND D2 = GENERAL-PURPOSE GERMANIUM DIODES
IC1 AND IC2 = CD4001

C_2 = 1 μF, p = 10 ms - 100 ms
C_2 = 0·1 μF, p = 1 ms - 10 ms
C_2 = ·01 μF, p = 100 μs - 1 ms
C_2 = 1000 pF, p = 10 μs - 100 μs
C_2 = 100 pF, p = 1 μs - 10 μs

Fig. 2.29. Simple high-quality variable (1 μs to 100 ms) pulse generator

triggers the second monostable (built around IC_2), which thus gives a delayed output pulse. With S_1 in the 'direct' position the IC_2 monostable fires at the same time as IC_1, and the circuit thus gives a non-delayed output.

The simple pulse-generator circuits of *Figure 2.26 and 2.27* are not suitable for commercial manufacture, for two main reasons. The first of these is that, since the period of a basic COS/MOS monostable multivibrator is determined by the transfer-voltage value of the individual COS/MOS i.c. as well as by the circuits' time-constant values, the circuits cannot be manufactured to give specific time-period ranges unless component values are individually selected. This particular snag can be overcome by modifying the basic monostable circuit as shown in *Figure 2.28*.

Here, R_3 and R_4 are wired as an adjustable potential divider across the supply lines, and the circuit's main timing resistor (series combination R_1 and R_2) is connected between timing capacitor C_1 and the slider of R_4. The effect of this modification is to enable the effective 'aiming' voltage of C_1, and hence the timing period of the circuit, to be varied via R_3, to compensate for variations of transfer voltage from one i.c. to another. The performance of this 'compensatable' circuit can thus be made independent of the CD 4001 characteristics. Note that the circuit must be used with a stabilised power supply, since the pulse length is influenced by supply variations.

The second reason that the simple *Figure 2.26 and 2.27* circuits are not suitable for commercial manufacture is that the periods of their monostable pulses are influenced by as much as 20 per cent by the shapes and frequencies of their input trigger signals. Specifically, if the input trigger signal is still 'high' at the time that the generated pulse is due to terminate, the period of the pulse may be increased by as much as 20 per cent. In most amateur applications this variation of pulse length is of no importance, but in commercial applications it may be quite unacceptable.

Fortunately, the pulse-length variation mentioned above does not occur if the monostable is triggered via a pulse waveform that has a length significantly less than the desired output pulse length. *Figure 2.29* shows how this fact can be turned to advantage to make a high-quality variable pulse generator with excellent stability.

Here, two of the gates of IC_1 are wired as a simple fixed-period monostable pulse generator that is directly activated by the input trigger signal. This monostable gives an output pulse with a duration of 300 ns or so, and this brief pulse is used to provide the trigger signal to a monostable of the type described in *Figure 2.28*, which is built around IC_2, and which gives any pulse length in the range 1 μs

to 100 ms, depending on the value of C_2. The length of the pulse is variable over a decade range via R_4 with any given value of C_2.

This pulse is generated in synchrony with the original input signal, but is directly triggered by a pulse with a fixed length of 300 ns, irrespective of the shape of the original input trigger waveform. Since the 300 ns pulse is short relative to any of the pulse lengths at the output of the circuit, the output pulse lengths are not influenced by the shape of the original input trigger signals, and the circuit acts as a high-quality pulse generator. This generator is intended to be used in conjunction with an existing external-trigger waveform generator. Note that the output of this pulse generator is of fixed amplitude, and is intended to feed into fairly high impedance loads.

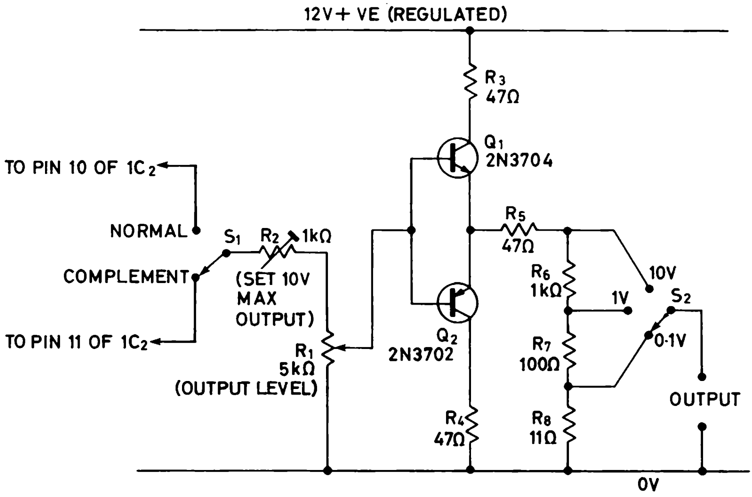


Fig. 2.30. Add-on output stage for use with Fig. 2.29 circuit gives low-impedance, variable-amplitude output signals

Figure 2.30 shows an add-on circuit that can be used in conjunction with the circuit of *Figure 2.29* to enable its output pulse amplitude to be made fully variable from zero to ten volts at an impedance level suitable for feeding into low impedance loads. The add-on circuit can readily be adapted for use with any of the *Figure 2.23 to 2.28* circuits.

In the add-on circuit of *Figure 2.30* the output of the pulse generator is fed to 'level' control R_1 via selector switch S_1, which enables either a 'normal' or a 'complement' pulse output to be selected. The output of the 'level' control is fed to complementary emitter follower Q_1-Q_2 and thence on to the circuit's output terminals via a simple three-position

decade attenuator. The peak output level of the circuit is 10 V, and the output pulses have typical rise and fall times of less than 50 ns. The circuit (and the pulse generator) must be powered from a 12 V regulated supply, and typically draws a current of only a couple of milliamps.

Type 555 pulse-generator circuits

The '555 timer' i.c. mentioned earlier in this chapter is specifically designed to give a monostable timing action, and acts as an excellent pulse generator; it can generate pulses with periods ranging from 5 μs to several hundred seconds, and can be triggered at frequencies up to about 100 kHz. Its output pulses have typical rise and fall times of 100 nanoseconds, and are available at a low impedance level. The pulse timing periods are virtually independent of supply-rail voltage and thermal variations.

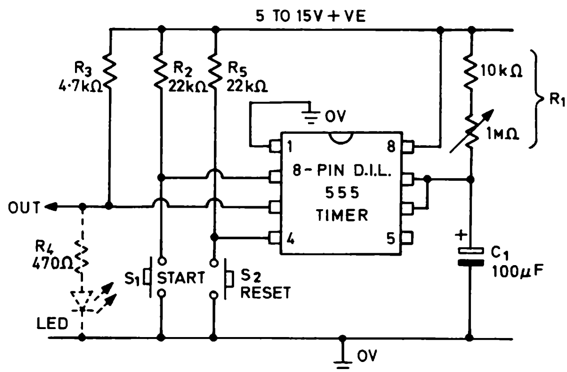


Fig. 2.31. Manually triggered 555 variable (1.1 to 110 second) pulse generator, with reset facility

Figure 2.31 shows the practical circuit of a manually-triggered 555 variable (1.1 to 110 second) pulse generator, which has a manual 'reset' facility and has provision for a visual (LED) output. The action of this circuit (and all other 555 circuits described in this section) is such that 'start' and 'reset' pins 2 and 4 are normally biased high, and output pin 3 is normally at ground volts. The monostable timing action is initiated or triggered by momentarily driving pin 2 of the i.c. below $\frac{1}{3} V_{CC}$ (by briefly closing 'start' button S_1).

As soon as this trigger signal is applied, the pin-3 output of the i.c. goes high and C_1 starts to charge exponentially towards the supply-rail

voltage (V_{cc}) via R_1. After a delay determined by the C_1 and R_1 values, the C_1 voltage rises to $\frac{2}{3}V_{cc}$; at this point the monostable action terminates, and the output pulse (at pin 3) switches abruptly to the low state again. The timing period, t, of the circuit equals $1.1 \times C_1 \times R_1$, where t is in milliseconds, C_1 is in microfarads, and R_1 is in kilohms. Note that the timing periods of the circuit can be terminated prematurely, if required, by briefly driving pin 4 of the i.c. below $\frac{1}{3}V_{cc}$ by momentarily closing 'reset' button S_2.

The *Figure 2.31* circuit can be triggered electronically by eliminating S_1 and S_2 and feeding a suitable trigger pulse to pin 2 of the i.c. This trigger pulse must be negative-going, with an amplitude that switches from an 'off' value greater than $\frac{2}{3}V_{cc}$ to an 'on' value less than $\frac{1}{3}V_{cc}$, and with a width that is greater than 100 ns but less than the desired output pulse, so that the trigger pulse is removed by the time the monostable period terminates.

C1 VALUE	PULSE WIDTH RANGE
10μF	90 ms – 1·2 sec
1μF	9 ms – 120 ms
0·1μF	0·9ms – 12 ms
·01μF	90μs – 1·2 ms
·001μF	9μs – 120μs

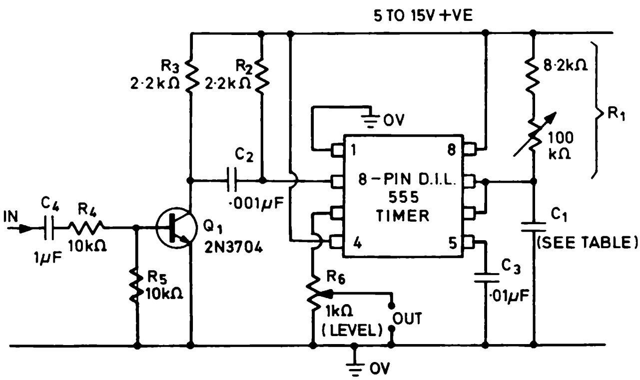


Fig. 2.32. Simple add-on pulse generator, triggered by rectangular input signals; circuit can be used at trigger frequencies up to 100 kHz

Figure 2.32 shows the circuit of a simple add-on pulse generator that generates pulses in the range 9 μs to 1.2 seconds and is triggered by externally-applied rectangular input signals. Here, the input signals are applied to Q_1 base via C_4 and R_4, and Q_1 amplifies the input signal and converts it into a suitable trigger form via C_2 and R_2. The

pulse periods of the circuit are fully variable via C_1 and R_1, and the output pulse amplitude is fully variable via R_6.

An alternative add-on 555 pulse generator, which can be triggered by any shape of input waveform, is shown in *Figure 2.33*. Here, IC_1 is wired as a Schmitt trigger, which converts any pin-2 input waveform into a pin-3 rectangular output waveform; this output waveform is

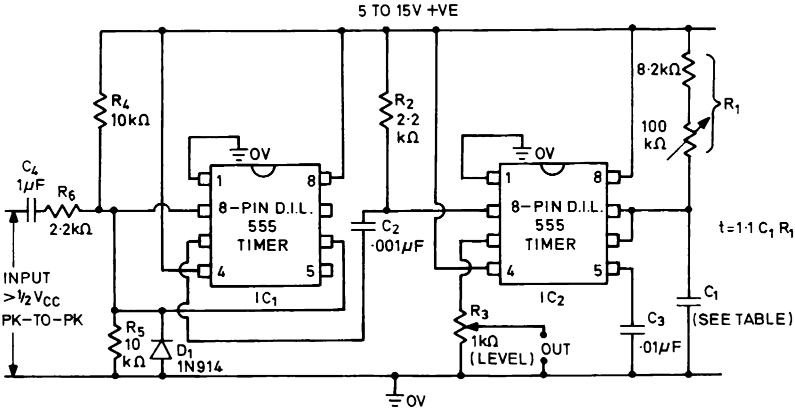


Fig. 2.33. Improved add-on pulse generator, triggered by any input waveform

converted into a form suitable for triggering the IC_2 monostable via C_2 and R_2. The only requirement of the initial input waveform is that its peak-to-peak amplitude must be greater than $\frac{1}{2}V_{cc}$.

Finally, *Figure 2.34* shows how a second 555 monostable stage can be added to the *Figure 2.33* circuit to make an add-on delayed-pulse generator. The 'delay' period of the circuit is determined by C_1 and R_1, and the 'width' period is determined by C_7 and R_9. Both periods are fully variable from 9 μs to 1.2 seconds.

Type 74121N TTL pulse-generator circuits

All the i.c. pulse-generator circuits that we have looked at so far in this chapter produce useful waveforms, but are incapable of producing pulses with lengths less than a few microseconds. TTL (transistor-transistor logic) pulse-generator integrated circuits capable of generating pulses with lengths down to a few tens of nanoseconds are readily available, however, and should be used when very narrow pulses or pulses with rise and fall times down to a few nanoseconds are required. A TTL i.c. of particular interest in this respect is the device known as the 74121N monostable multivibrator.

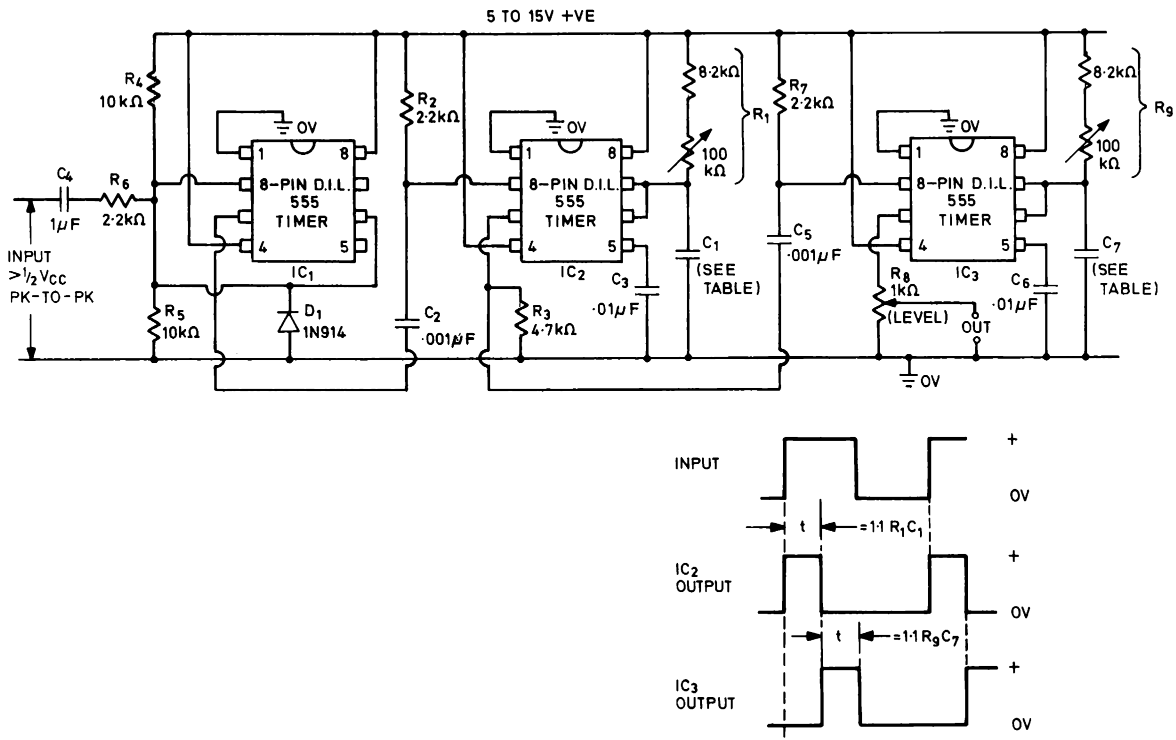


Fig. 2.34. Add-on delayed-pulse generator, triggered by any input waveform; for C_1 (and C_7) values see table in Fig. 2.32

Figure 2.35 shows the outline, pin notations, and simplified internal circuit of the 74121N i.c. The device can be triggered on either the leading or trailing edges of an input waveform, has three alternative input trigger terminals, and produces both Q and $\bar{Q}$ (in-phase and anti-phase) outputs. The i.c. can be made to produce fixed pulses of about 30 ns width by using built-in timing components, or can be made to produce pulse widths from a few tens of nanoseconds up to a few tens of seconds by using external timing components.

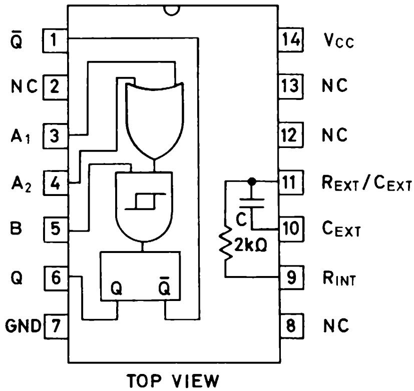


Fig. 2.35. Outline, pin notations and simplified internal circuit of 74121N monostable multivibrator i.c.

Dealing first with methods of triggering the i.c., *Figures 2.36a and b* show two basic ways of firing the device when it is connected as a simple 30 ns pulse generator using internal timing components. In the *Figure 2.36a* circuit the input signal is applied to trigger pin 5 via a transistor buffer stage. Pin 5 is known as the B input terminal of the i.c., and is internally connected as a Schmitt trigger that fires the monostable on the leading or rising edge of the input waveform if pins 3 (A_1) and/or 4 (A_2) are low or at logic 0 at this time. Note that slow-rising edges can be used to trigger the monostable via the B input terminal.

Figure 2.36b shows how to connect the i.c. so that it triggers on the falling or trailing edge of the input waveform. Here, the input signal is fed to pin 3 (A_1) and 4 (A_2) of the i.c. via a type 7413N Schmitt trigger, which produces the sharp rise and fall times required to correctly operate the A_1 and A_2 inputs. A_1 and A_2 are negative-edge triggered logic inputs, and trigger the monostable when either or both go to logic 0 with input B disconnected or biased at logic 1.

Note from the above brief description of the triggering inputs that these inputs can be used in a variety of ways to give different forms of

trigger action. A_1 and A_2 can, for example, be used to give trailing-edge OR logic triggering with input B used to give 'enable' or 'disable' action, or input B can be used to give leading-edge triggering with A_1 and A_2 used to give 'enable' and 'disable' action.

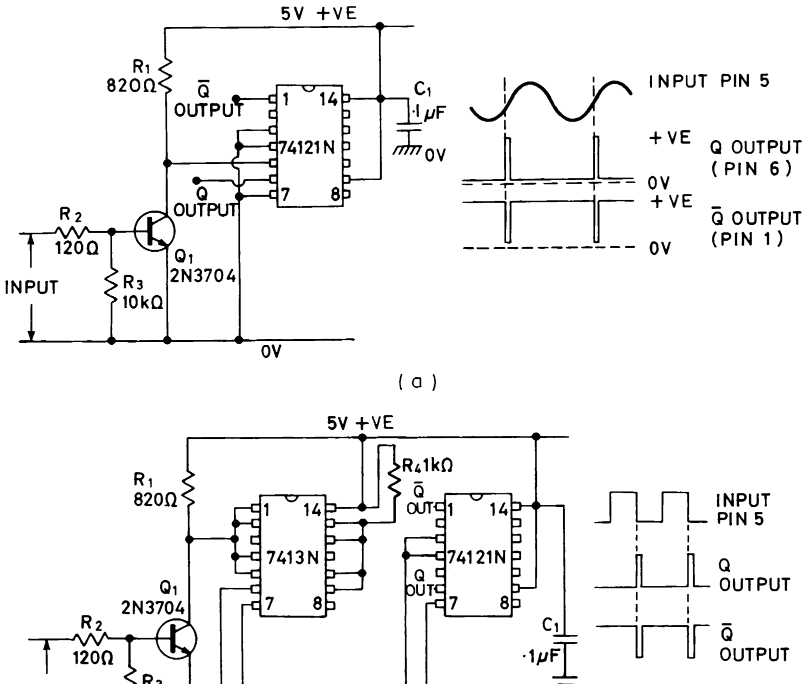


Fig. 2.36. 30 ns pulse generator: (a) using B input leading-edge triggering; (b) using A_1 and A_2 input trailing-edge triggering

Dealing next with the timing circuitry of the i.c., *Figures 2.37a to c* show a number of alternative ways of obtaining desired pulse lengths from the device. The i.c. has three externally-available timing-component terminals. A low-value timing capacitor is built into the i.c., and can be augmented by connecting an external timing capacitor between pins 10 and 11. This capacitor can have any value from a few picofarads to thousands of microfarads. If polarised timing capacitors are used, their positive terminals must be connected to pin 11.

The i.c. incorporates a fixed-value (nominally 2 kΩ) built-in timing resistor, which can be utilised by wiring pin 9 directly to positive-supply pin 14. Alternatively, an external timing resistor, with a maximum value of 40 kΩ, can be wired between pins 9 and 14, to give a total timing-resistance value equal to the sum of the internal and external resistance

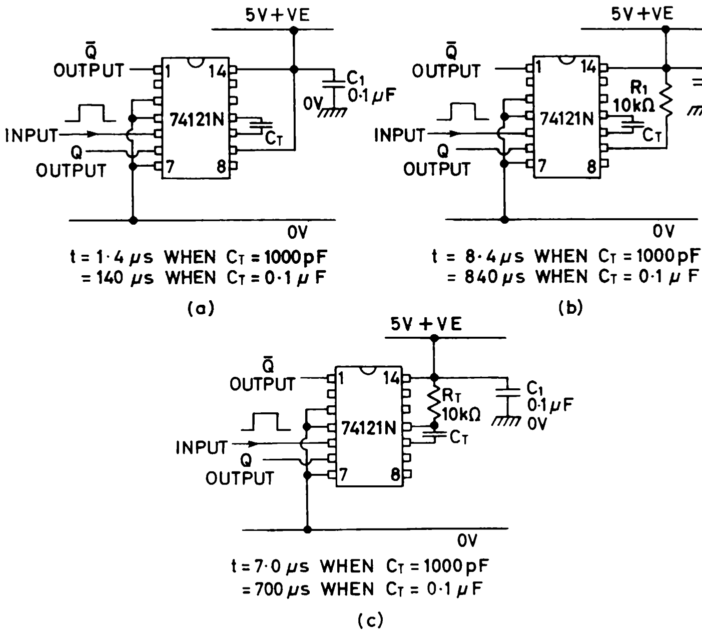


Fig. 2.37. Pulse generator using external timing capacitor and (a) internal timing resistor or (b) internal and external timing resistors or (c) external timing resistor

values. Finally, the internal resistor can be ignored completely, and an external timing resistor, with a value in the range 1.4 kΩ to 40 kΩ, can be wired between pins 11 and 14. Whichever timing connection is used, the output pulse width = $0.7R_T C_T$, where the width is specified in milliseconds, R_T is the total timing resistance in kilohms, and C_T is the timing capacitance in microfarads.

The four basic ways of using the timing circuitry of the 74121N i.c. are illustrated in *Figures 2.36 and 2.37*. In the *Figure 2.36a and b* circuits no external timing capacitor is used, and the internal timing resistor is used by connecting pins 9 and 14 directly together. This circuit generates a pulse width of about 30 ns.

The *Figure 2.37a* circuit uses the built-in timing resistor of the i.c. in conjunction with an external timing capacitor connected between

pins 10 and 11. The circuit generates a pulse width of about 1.4 μs when C_1 has a value of 1000 pF, and a width of 140 μs when C_1 has a value of 0.1 μF.

The *Figure 2.37b* circuit uses an external timing resistor in series with the internal timing resistor of the i.c., in conjunction with an external timing capacitor. The circuit generates a pulse width of about 840 μs when a 10 kΩ external resistor is used in conjunction with a 0.1 μF timing capacitor.

Finally, the *Figure 2.37c* circuit ignores the internal timing resistor of the i.c., and uses an external timing resistor connected between pins 11 and 14 in conjunction with an external timing capacitor. This circuit generates a pulse width of about 700 μs when a 10 kΩ resistor is used in conjunction with a 0.1 μF timing capacitor.

The basic *Figure 2.37c* circuit is of particular value in decade-ranged variable pulse generator applications, and *Figure 2.38* shows how it can be adapted to act as a high-performance add-on pulse generator that covers the range 100 ns to 100 ms in six decade ranges.

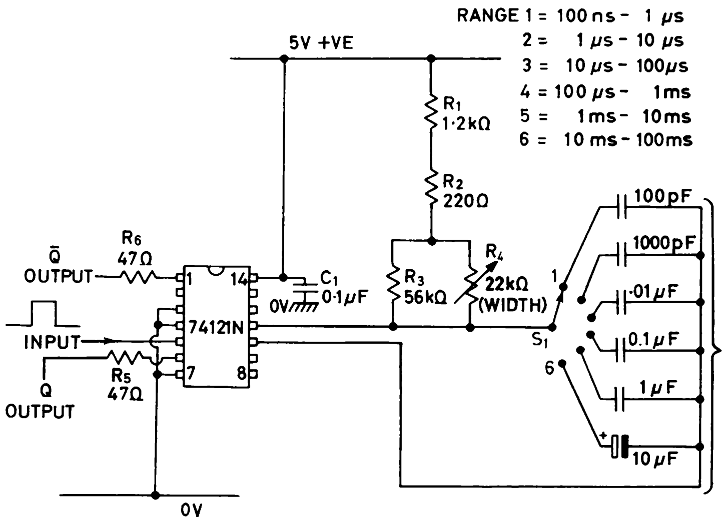


Fig. 2.38. High-performance add-on pulse generator covering the range 100 ns to 100 ms

To complete this chapter, *Figure 2.39* shows how two of the *Figure 2.38* circuits can be coupled together to make a wide-range delayed pulse generator of the add-on type. Note that both these generator circuits give inverted and non-inverted outputs of fixed amplitude. Each output is protected against short circuit damage via a 47 Ω series resistor.

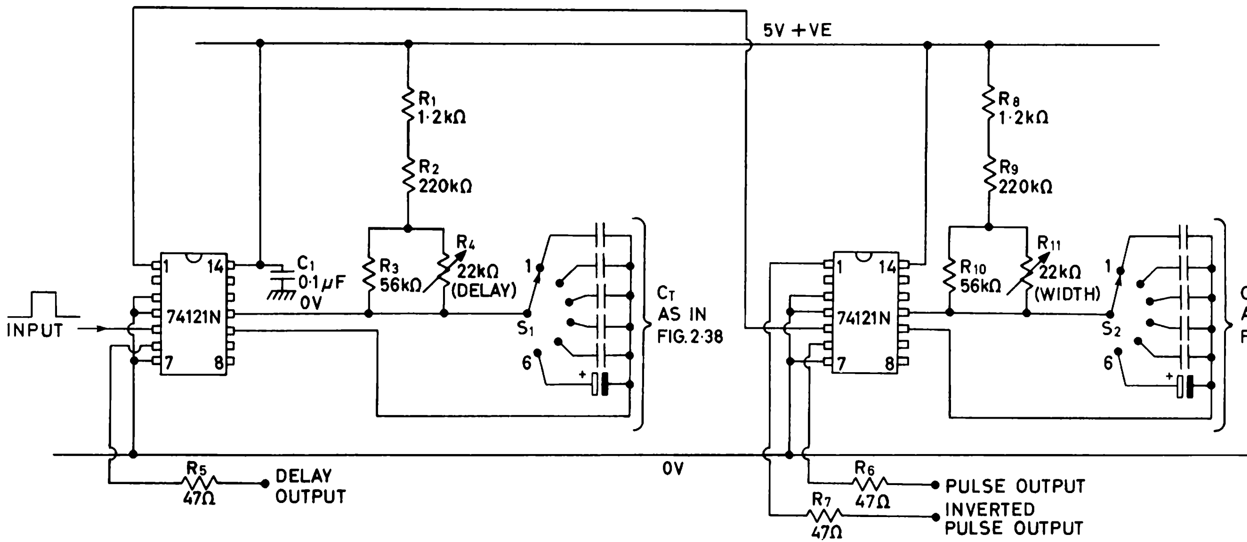


Fig. 2.39. High-performance add-on delayed pulse generator covering the range 100 ns to 100 ms

CHAPTER 3

TRIANGLE, RAMP AND SAWTOOTH GENERATORS

Triangle, ramp and sawtooth waveforms have a variety of uses in electronics, and can be generated in a variety of ways. Triangle waveforms are particularly useful for checking crossover distortion in audio amplifiers. Ramp waveforms can be used to amplitude- or frequency-modulate audio signals to produce special effects. Sawtooth waveforms can be used as timebases for oscilloscopes and wobbulators. A variety of practical waveform generators of all three types are described in this chapter.

U.J.T. sawtooth generators

The unijunction transistor (u.j.t.) is a special-purpose device that is particularly suitable for generating sawtooth waveforms. *Figure 3.1* shows the practical circuit of a simple wide-range (25 Hz–3 kHz) u.j.t. circuit that produces a non-linear sawtooth waveform. The circuit action is such that C_1 charges exponentially towards the positive supply rail via R_1–R_2 until the C_1 voltage reaches the 'peak point' or firing voltage of the u.j.t., at which point the u.j.t. turns on and rapidly discharges C_1. As soon as C_1 is effectively discharged, the u.j.t. turns off again, C_1 starts to recharge via R_1–R_2, and so the sequence repeats *ad infinitum*.

Thus a repetitive non-linear (exponential) sawtooth is developed across C_1 in the *Figure 3.1* circuit, and this sawtooth can be fed to external circuits via potentiometer R_5 and buffer transistors Q_2–Q_3. With the component values shown, the frequency range of the circuit is variable from about 25 Hz to 3 kHz via R_1. The operating frequency

can be varied from less than one cycle per minute to over 100 kHz by changing the C_1 value. Reducing the C_1 value increases the frequency, and vice versa.

The u.j.t. circuit can be made to generate a linear sawtooth waveform by charging its timing capacitor (C_1) from a constant-current source, as

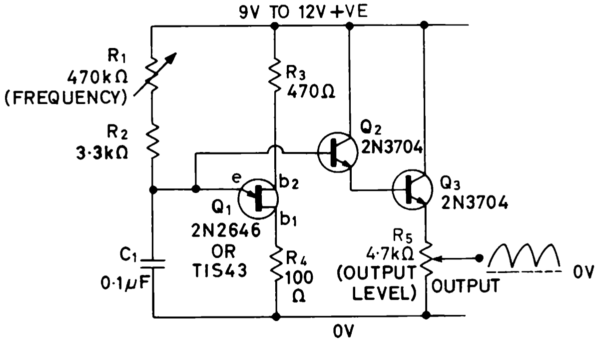


Fig. 3.1. Simple wide-range (25 Hz to 3 kHz) u.j.t. circuit produces non-linear sawtooth waveform

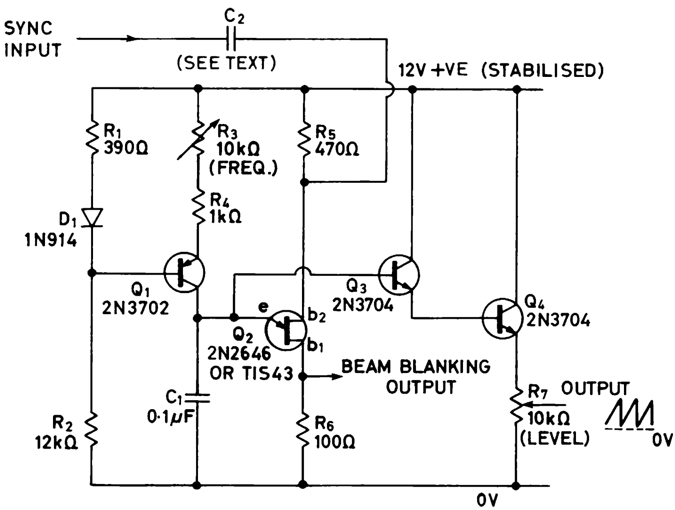


Fig. 3.2. Linear u.j.t. sawtooth generator can be used as simple oscilloscope timebase

shown in *Figure 3.2.* This circuit can be used as an oscilloscope timebase. Here, Q_1 is used as a temperature-compensated constant-current generator, with current variable over the approximate range 35 μA to 390 μA via R_3. The linear sawtooth of C_1 is available externally via

potentiometer R_7 and buffer transistors Q_3–Q_4. With the component values shown, the operating frequency is variable over the range 60 Hz to 700 Hz. Alternative frequencies can be obtained by changing the C_1 value.

The *Figure 3.2* circuit is suitable for use as a simple timebase generator for an oscilloscope. In this application the output of the circuit should be taken to the external timebase socket of the oscilloscope, and positive 'flyback' pulses from R_6 can be taken via a high-voltage blocking capacitor and used for beam blanking. The generator can be synchronised to an external signal by feeding the external signal to Q_2 via C_2. This signal, which should have a peak amplitude of between 200 mV and 1 V, effectively modulates the supply voltage (and thus the triggering point) of Q_2, thus causing Q_2 to fire in synchrony with the external signal.

C_2 should be chosen to have a lower impedance than R_5 at the sync signal frequency, and must have a working voltage greater than the external voltage from which the signal is applied. If the sync signal takes a rectangular form, with short rise and fall times, C_2 can simply be given a value of a few hundred picofarads.

Op-amp triangle and ramp generators

Operational amplifiers can readily be made to produce low-frequency triangle and ramp waveforms for purposes such as testing audio amplifiers for crossover distortion, etc. The easiest way to generate a ramp or triangle waveform is to use the simple op-amp relaxation oscillator (IC_1) and voltage follower output (IC_2) circuit shown in *Figure 3.3*. The basic relaxation oscillator was described in Chapter 2 as a square-wave generator; the circuit action is such that C_1 first charges exponentially in a positive direction via R_1 and R_2 until a certain firing voltage is reached, at which point the op-amp switches regeneratively and C_1 starts to charge exponentially in the negative direction via R_1 and R_2 until a second firing voltage is reached, at which point the op-amp switches regeneratively back to its original state, and the sequence repeats *ad infinitum.* A square-wave signal is generated at pin 6 of IC_1, and an approximately triangular waveform is generated across C_1. The C_1 triangle waveform is made available for external use via potentiometer R_5 and voltage-follower buffer stage IC_2.

In the *Figure 3.3* circuit the peak-to-peak amplitude of the output triangle signal is limited to about 1.7 V via the R_3–R_4 potential divider to ensure that the waveform is derived from a reasonably linear section of the exponential charging waveform of C_1. R_1 enables the frequency to be varied between roughly 800 Hz and 8 kHz. Alternative frequencies

can, of course, be obtained by using alternative values of C_1. The output level of the circuit is fully variable via R_5.

The *Figure 3.3* circuit generates a symmetrical triangle waveform, since its main timing capacitor charges in both positive and negative directions via the same resistance network. *Figure 3.4* shows how the

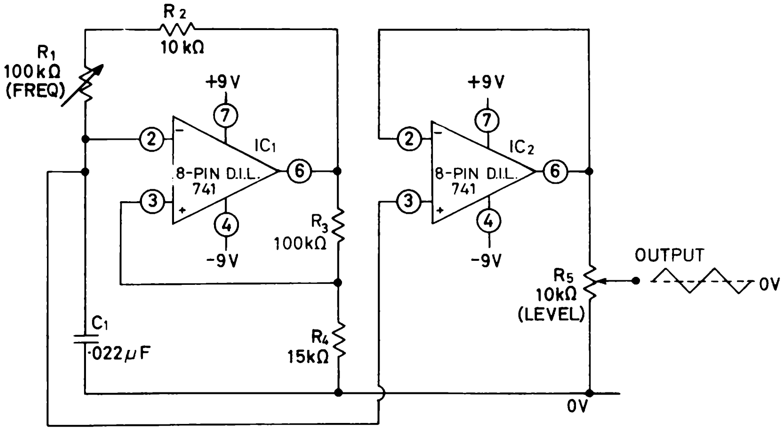


Fig. 3.3. Simple 800 Hz–8 kHz op-amp triangle generator

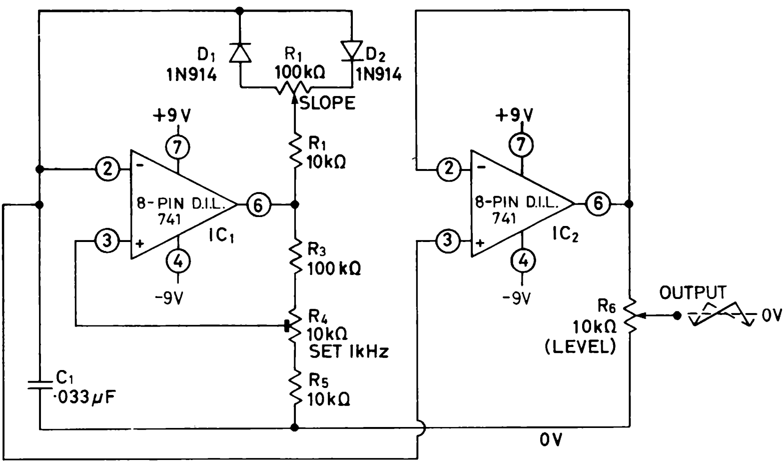


Fig. 3.4. 1 kHz variable-slope op-amp ramp generator

above circuit can be modified as a fixed-frequency (1 kHz) variable-slope ramp generator. The slopes of the output waveform are controlled by R_1. The period of the complete waveform is fixed at 1 ms, and R_1 enables the rising (or falling) part of the slope to be varied from roughly

0.09 ms to 0.9 ms. The frequency is variable over a very limited range via R_4, which enables the frequency to be set to precisely 1 kHz. The output signal amplitude is fully variable via R_6.

The simple triangle and ramp generator circuits of *Figures 3.3 and 3.4* generate their waveforms directly from timing capacitor C_1. Since this capacitor is charged exponentially, the output waveforms are inevitably slightly non-linear, the degree of non-linearity being proportional to the amplitude of the output signals. A superior system of generating a triangle waveform is shown in *Figure 3.5*. This circuit generates a waveform with excellent linearity over the frequency range 100 Hz to 1 kHz

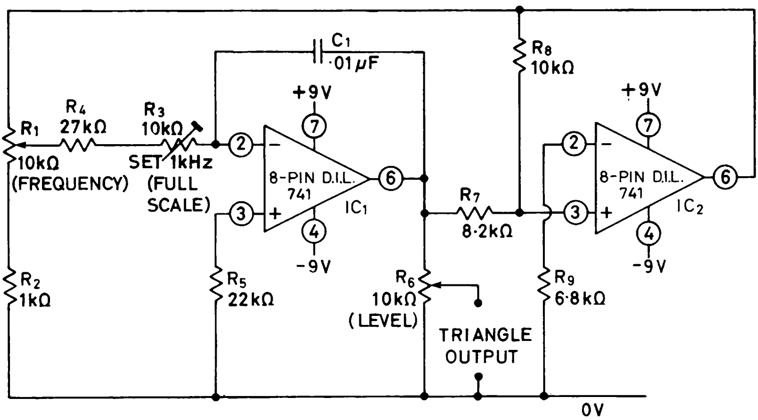


Fig. 3.5. 100 Hz to 1 kHz linear triangle generator

with the component values shown. The frequency range can readily be extended by using alternative values of C_1.

The *Figure 3.5* circuit is made up of two sections, these being an integrator (IC_1) and a differential voltage comparator switch (IC_2). The integrating network, which is built around IC_1, comprises R_3–R_4 and C_1, and is driven from variable potential divider R_1–R_2, which in turn is driven from the output of voltage switch IC_2. The triggering level of IC_2 is determined by the ratios of R_7 and R_8. The circuit action is such that C_1 is charged in alternately positive and negative directions via R_3–R_4 and potential divider R_1–R_2 in such a way that a perfectly linear and symmetrical triangle waveform is produced at output pin 6 of IC_1. This waveform is made available for external use via potentiometer R_6. The operating frequency of the circuit can be varied over a full decade range via R_1, and can be set to precisely 1 kHz full-scale via R_3. Alternative frequency ranges can be obtained by changing the C_1 value. Increasing the C_1 value lowers the frequency, and vice versa.

Figure 3.6 shows how the above circuit can be modified so that it produces a variable-slope linear ramp waveform. The two circuits are similar, except that the integrator charging network of the *Figure 3.6* circuit contains steering diodes D_1 and D_2 and variable resistor R_4. These components enable the positive and negative charging time

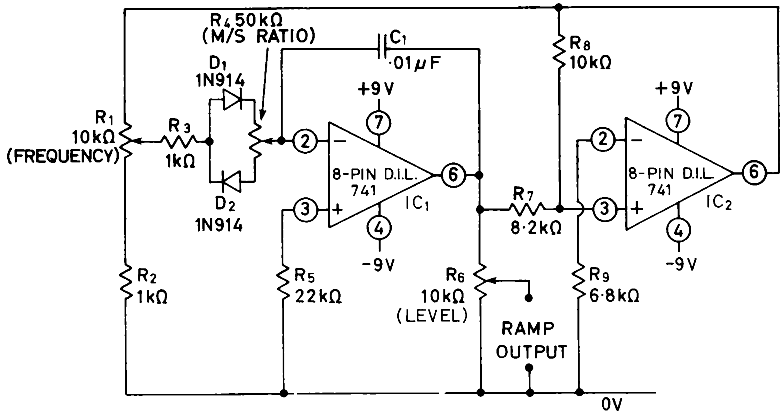


Fig. 3.6. 100 Hz to 1 kHz variable-slope linear ramp generator

constants of C_1 to be varied relative to one another. On positive half-cycles C_1 charges via R_3–D_1 and the upper half of R_4, and on negative half-cycles C_1 charges via R_3–D_2 and the lower half of R_4. R_4 thus enables the relative durations of the positive and negative slopes of the ramp waveform to be varied without appreciably effecting the operating frequency of the circuit. The operating frequency is independently variable via R_1 and the output level is variable via R_6.

Type 555 triggered sawtooth generators

The type 555 timer i.c. can be made to generate a triggered non-linear (exponential) sawtooth waveform by connecting it as shown in *Figure 3.7*. Here, the circuit is basically connected as a triggered monostable multivibrator, except that the output waveform is taken from across timing capacitor C_1 via buffer transistors Q_2–Q_3 and potentiometer R_7. The circuit action is such that the C_1 voltage (and the output voltage) is normally at zero volts, but each time the circuit is triggered C_1 charges exponentially via R_1 and R_2 to $\frac{2}{3}V_{CC}$, at which point the monostable period terminates. The period of the sawtooth waveform can be varied over the range 9 μs to 1.2 seconds by using the C_1 values

indicated in the table of *Figure 3.7*. The maximum usable repetition frequency of the circuit is approximately 100 kHz.

Note that this circuit must be triggered via rectangular input waveforms with reasonably short rise and fall times. The sawtooth period is variable over a decade range via R_2, and the amplitude of the output waveform is fully variable via R_7.

The basic *Figure 3.7* circuit can be made to produce a triggered linear sawtooth waveform by charging C_1 via a constant-current generator, as shown in the circuit of *Figure 3.8*. Here, Q_1 is used as the constant current generator, and the output waveform is taken from across C_1 via Q_2 and potentiometer R_6.

When a capacitor is charged via a constant-current generator, the voltage across the capacitor rises linearly at a predictable rate that can be expressed as:

$$\text{Volts per second} = I/C$$

where I is expressed in amps and C is expressed in farads. Using more practical quantities, alternative expressions for the rate of voltage rise are:

$$\text{Volts per microsecond} = \text{amps}/\mu\text{F}$$

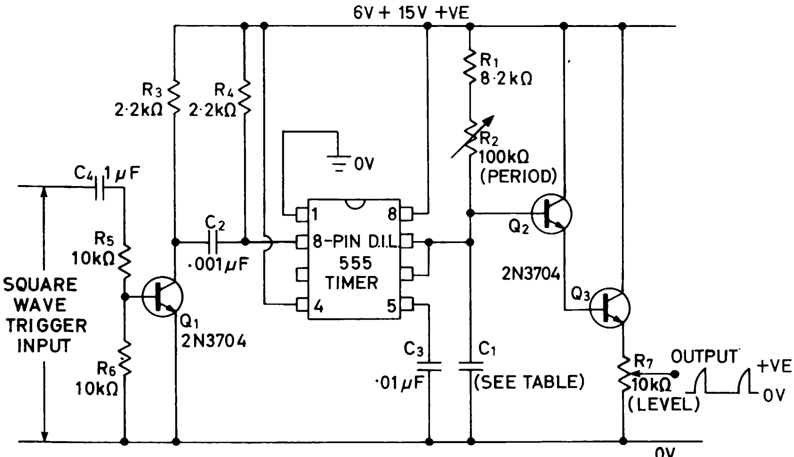
or:

$$\text{Volts per millisecond} = \text{mA}/\mu\text{F}$$

Note that the rate-of-rise of the voltage can be increased by increasing the charging current or decreasing the value of capacitance.

In the *Figure 3.8* circuit the charging current can be varied over the approximate range 90 μA to 1 mA via R_1, thus giving rates of rise on the 0.01 μF capacitor of 9 V/ms to 100 V/ms respectively. Now, remembering that each monostable cycle of the 555 i.c. terminates at the point when C_1 voltage reaches $^2/_3\,V_{cc}$, and assuming that a 9 V supply is used (giving a $^2/_3\,V_{cc}$ value of 6 V), it can be seen that the sawtooth cycles of the circuit have periods variable from 666 μs (= $^6/_9$ ms) to 60 μs (= $^6/_{100}$ ms) respectively. Periods can be increased beyond these values by increasing the C_1 value, or vice versa. Note when using this circuit that its supply rail must be stabilised if stable timing periods are to be obtained.

The *Figure 3.8* circuit can be used as the basis of a triggered oscilloscope timebase. The minimum useful ramp period that can be obtained from the circuit is about 5 μs, which, when expanded to give full deflection on a ten-division oscilloscope screen, gives a maximum timebase speed of 0.5 μs per division. Beam bright-up or blanking signals can be derived from the pin-3 output terminal of the type 555 i.c. The



C1 VALUE	SAWTOOTH PERIOD RANGE
10 μF	90ms – 1·2 sec
1 μF	9ms – 120 ms
0·1 μF	0·9ms – 12 ms
·01 μF	90 μs – 1·2 ms
·001 μF	9 μs – 120 μs

Fig. 3.7. Basic 555 triggered sawtooth generator

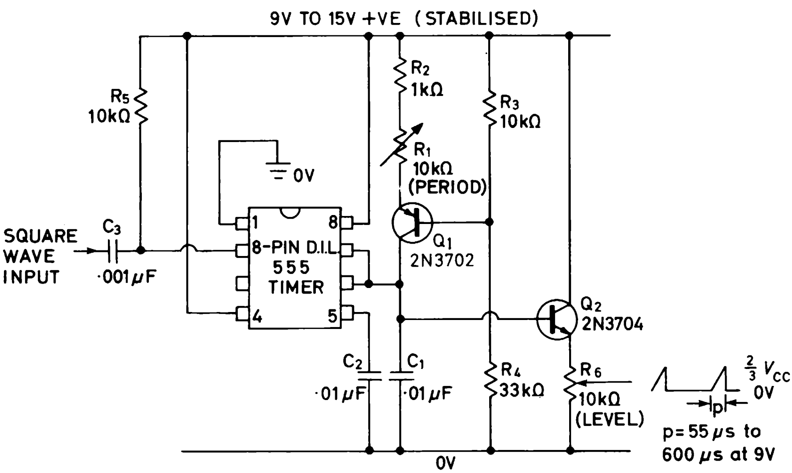


Fig. 3.8. Linear 555 triggered sawtooth generator

circuit gives excellent signal synchronisation at trigger frequencies up to about 150 kHz. The circuit must be triggered by rectangular input signals with reasonably short rise and fall times.

XR-2206 triangle and ramp generators

The XR-2206 function generator i.c. can readily be used to generate either linear triangle waveforms or variable-symmetry linear ramp waveforms. *Figures 3.9 to 3.12* show four practical examples of such circuits.

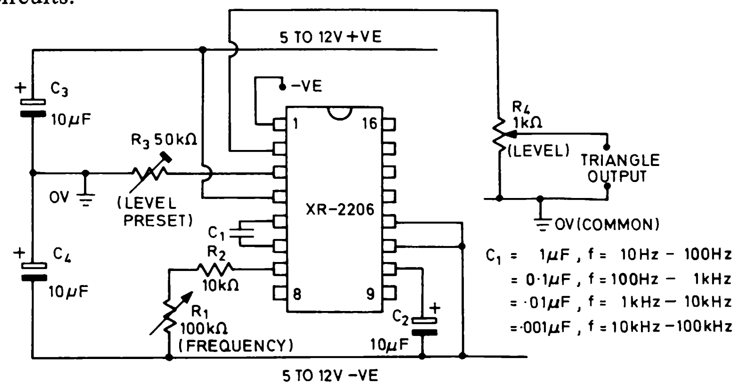


Fig. 3.9. XR-2206 split-supply triangle-wave generator

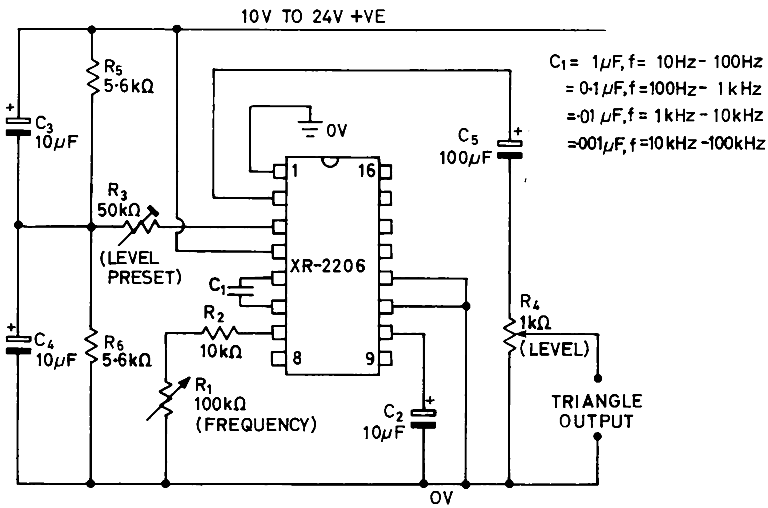


Fig. 3.10. XR-2206 single-supply triangle-wave generator

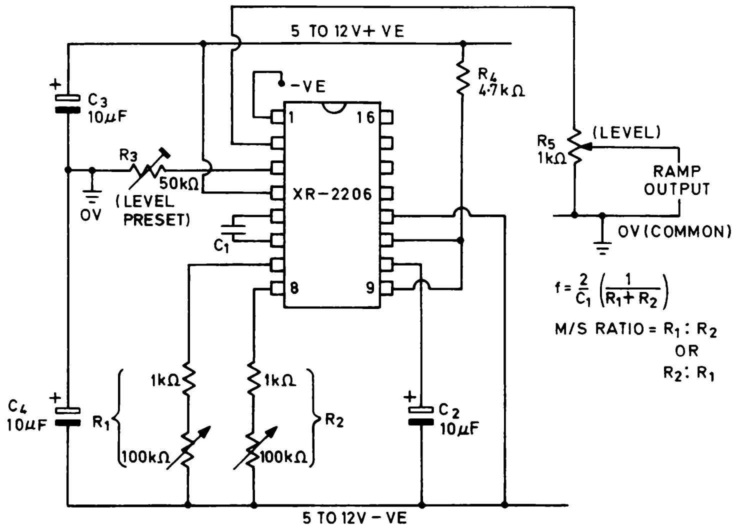


Fig. 3.11. XR-2206 split-supply variable-slope ramp generator

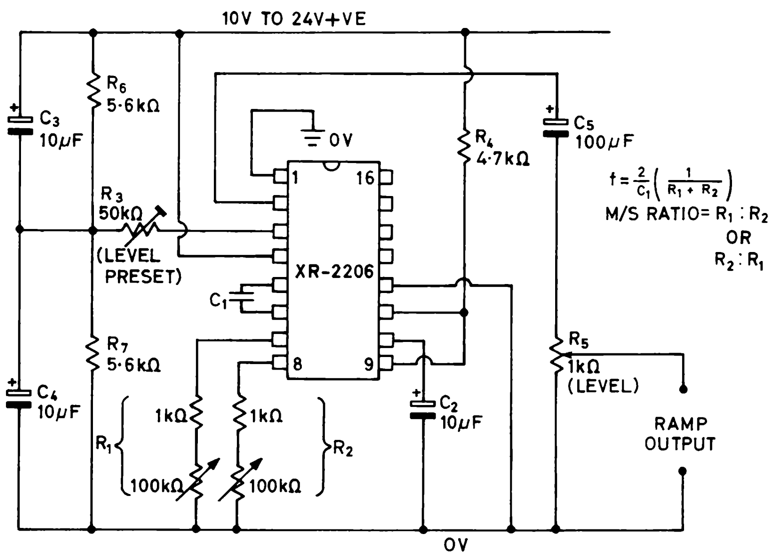


Fig. 3.12. XR-2206 single-supply variable-slope ramp generator

Figures 3.9 and 3.10 show the circuits of two alternative triangle wave generators. In each case the operating frequency is determined by the values of R_1–R_2 and C_1, and can be varied over a full decade range via 'frequency' control R_1. The frequency can be varied from 10 Hz to 100 kHz by using the indicated C_1 values. The *Figure 3.9* circuit is designed for split-supply (±5 V to ±12 V) operation, and the *Figure 3.10* circuit is designed for single-supply (10 V to 24 V) operation. Preset resistor R_3 in each circuit enables the maximum output level of the triangle wave to be preset to any desired level. The circuits can typically produce signals with unloaded amplitudes of about 12 V peak-to-peak before clipping occurs when they are used with ±9 V or 18 V supplies. Once R_3 has been preset, the output signal levels can be fully varied from zero to maximum via 'level' control R_4.

Figures 3.11 and 3.12 show the circuits of two alternative variable-slope linear ramp generators. The action of each circuit is such that timing capacitor C_1 is alternately charged linearly via R_1 and discharged linearly via R_2. Consequently the rising and falling slopes of the ramp are independently controlled. The symmetry or mark/space ratio (and thus the frequency) of the waveform can be varied over a 100 : 1 range via the R_1–R_2 controls.

The *Figure 3.11* circuit is designed for split-supply (±5 V to ± 12 V) operation, and the *Figure 3.12* circuit is designed for single-supply (10 V to 24 V) operation. As in the case of the XR-2206 triangle generator circuits, the maximum output levels of these circuits can be preset via R_3. The output levels are independently variable via R_5.

CHAPTER 4

MULTI-WAVEFORM GENERATORS

Each of the circuits we have looked at so far is designed to generate only a single specific type of waveform. The most useful types of generator, however, are those that can be made to generate a variety of waveform shapes, either simultaneously or alternatively via suitable 'mode' selection switching; A good range of practical 'multi-waveform' generator circuits is shown in this chapter.

Multi-waveform op-amp circuits

Figure 4.1 shows the practical circuit of an op-amp simultaneous sine-square generator that covers the frequency range 15 Hz to 15 kHz in three switch-selected variable decade ranges. Here, IC_1 is wired as a variable-frequency lamp-regulated Wien-bridge sine-wave oscillator of the type shown in *Figure 1.5*. Part of the sine-wave output of this oscillator is fed to the input of the second op-amp, IC_2, which is wired as a simple voltage comparator and has its other input terminal taken to the zero-volts line. The action of this i.c. is such that its output switches from positive saturation to negative saturation, or vice versa, each time the sine-wave input signal swings through the zero-volts level. This i.c. thus converts the sine-wave input signal to a square-wave output.

The *Figure 4.1* circuit is set up by simply adjusting R_5 to give approximately 2.5 V r.m.s. output at the maximum output setting of 'sine level' control R_6. Once set, the circuit generates a sine wave with a typical total harmonic distortion content of about 0.1 per cent. The square-wave output is available simultaneously with the sine wave, and has an amplitude that is variable via 'square level' control R_9 up to a

maximum peak-to-peak amplitude of about 15 V. The square-wave output swings symmetrically about the zero-volts level, and has typical rise and fall times of 1.5 μs and 0.5 μs respectively.

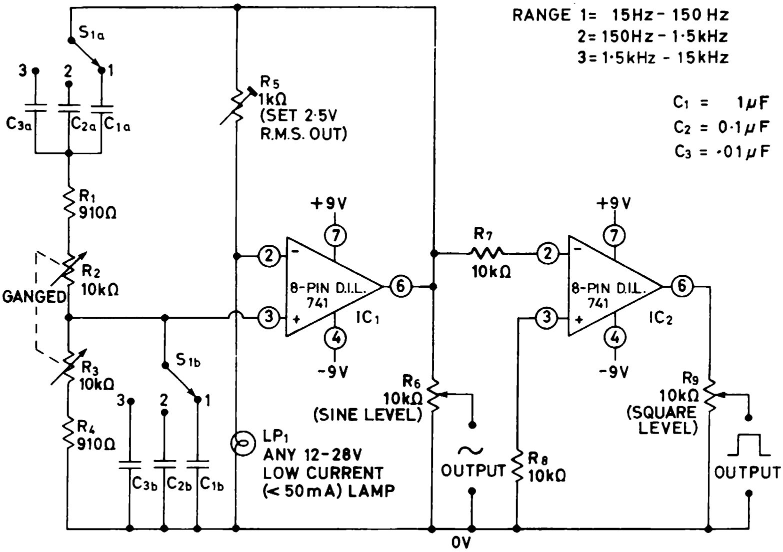


Fig. 4.1. 15 Hz to 15 kHz op-amp sine/square generator

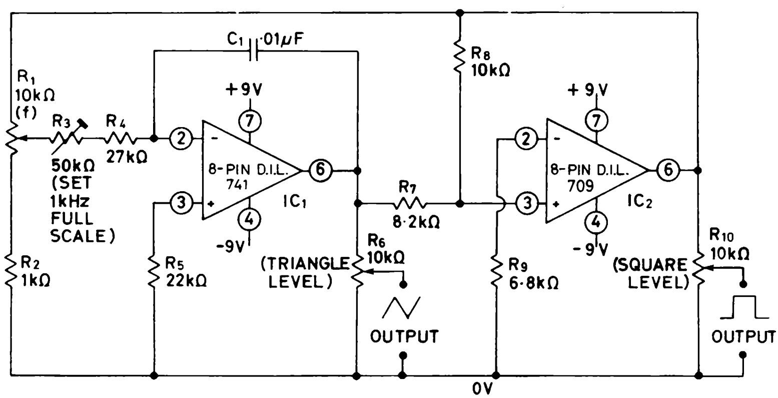


Fig. 4.2. 100 Hz to 1 kHz op-amp triangle/square generator

Figure 4.2 shows the practical circuit of an op-amp 100 Hz to 1 kHz triangle-/square-wave generator. This circuit simultaneously generates a linear and symmetrical triangle waveform across 'triangle level' control R_6 and a symmetrical square wave across 'square level' control R_{10}. The

square-wave output has typical rise and fall times of 1.5 μs and 0.5 μs respectively.

The *Figure 4.2* circuit is made up of two sections, these being an integrator (IC_1) and a differential voltage comparator switch (IC_2). The integrating network, which is built around IC_1, comprises R_3-R_4 and C_1, and is driven from variable potential divider R_1-R_2, which in turn is driven from the output of voltage switch IC_2. The triggering level of IC_2 is determined by the ratios of R_7 and R_8. The circuit action is such that C_1 is charged in alternately positive and negative directions via R_3-R_4 and potential divider R_1-R_2 in such a way that a perfectly linear and symmetrical triangle waveform is produced at output pin 6 of IC_1, and a square wave of identical frequency is produced at output pin 6 of IC_2. The operating frequency of the circuit can be varied over a full decade range via R_1, and can be set to precisely 1 kHz full-scale via R_3. Alternative frequency ranges can be obtained by changing the C_1 value. Increasing the C_1 value lowers the frequency, and vice versa.

The linear output triangle of the *Figure 4.2* circuit can be converted into a sine wave or into a variable mark/space ratio rectangular wave with the aid of suitable adaptor circuits. The circuit of a variable mark/space ratio adaptor is shown in *Figure 4.3*. Here, the op-amp is

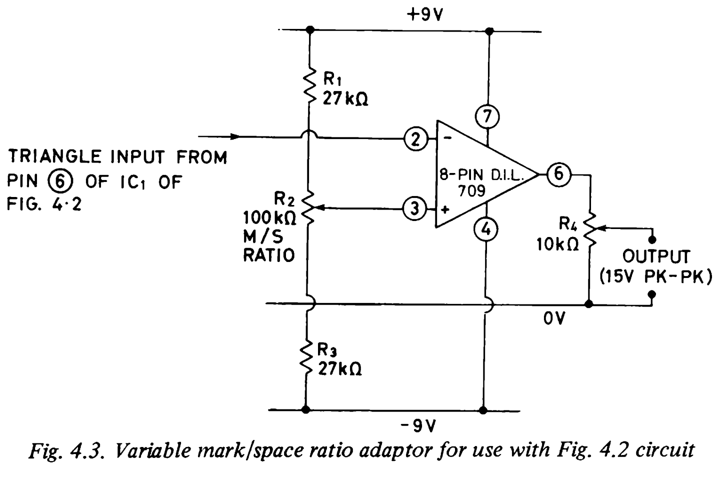


Fig. 4.3. Variable mark/space ratio adaptor for use with Fig. 4.2 circuit

wired as a simple voltage comparator, and has one input applied from the triangle output of the *Figure 4.2* circuit and the other input applied from a variable potential divider that is wired between the positive and negative voltage supply lines. The op-amp switches into positive or negative saturation each time the triangle voltage goes more than a few millivolts below or above the reference voltage set via R_2. By adjusting

the reference voltage, therefore, the op-amp can be made to change state at any point on the triangle waveform, and a variable mark/space ratio rectangular wave is thus available at the output of the op-amp.

The circuit of the sine-wave adaptor is shown in *Figure 4.4*. Here,

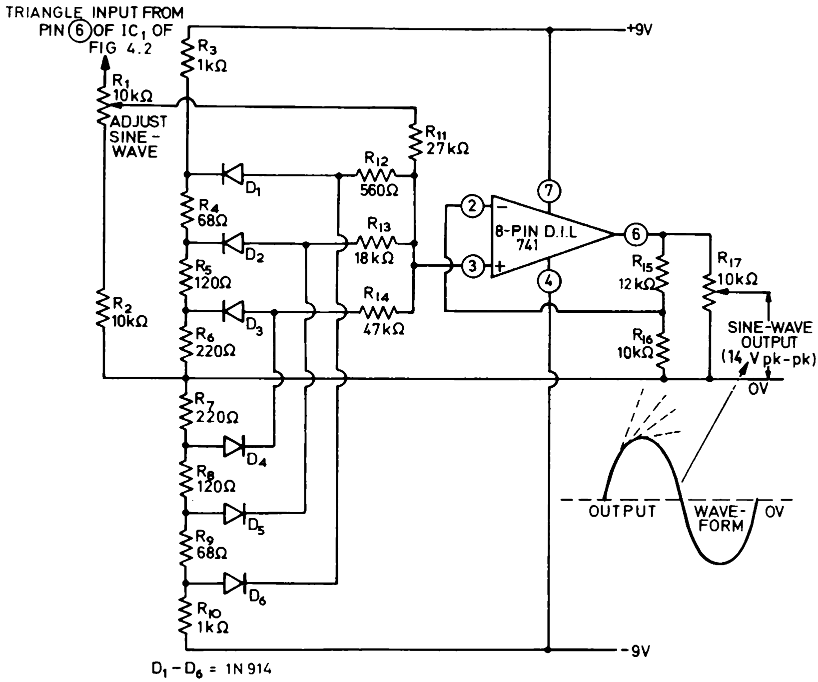


Fig. 4.4. Sine-wave adaptor for use with Fig. 4.2 circuit

the triangle waveform is fed into a resistor-diode matrix via adjustable potential divider R_1–R_2. The matrix converts the triangle waveform into a simulated sine wave by automatically reducing the slope of the triangle in a series of steps as the triangle amplitude increases. The resulting waveform is fed into a x 2.2 non-inverting d.c. amplifier, and is finally available with a maximum peak-to-peak amplitude of 14 V across variable output control R_{17}. As shown in the diagram, the final output waveform can be represented by a series of straight lines, there being four lines in each quarter-cycle. The waveform approximates a sine wave, and typically contains less than 2 per cent total harmonic distortion. R_1 should be adjusted to give the best sine-wave shape when the converter is initially connected to the *Figure 4.2* circuit.

Finally, *Figure 4.5* shows how the *Figure 4.2* circuit can be modified to produce a linear ramp waveform with a variable slope, or a square wave with a variable mark/space ratio. The two circuits are similar, except that the integrator charging network of the *Figure 4.5* circuit

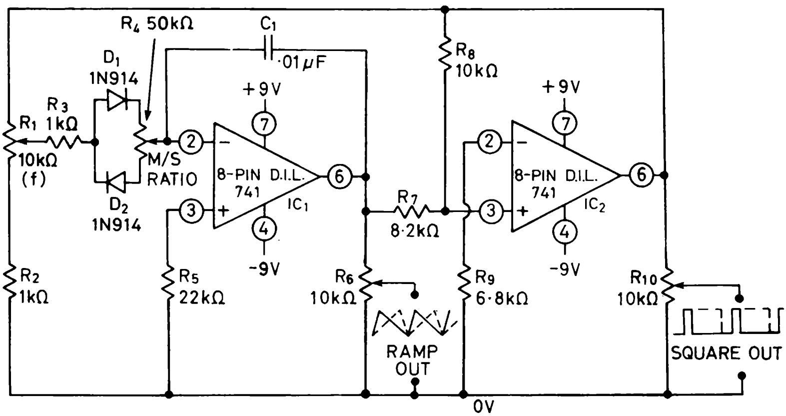


Fig. 4.5. 100 Hz to 1 kHz ramp/square generator with variable slope or M/S ratio

contains steering diodes D_1 and D_2, and variable resistor R_4. These components enable the positive and negative charging time constants of C_1 to be varied relative to one another. On positive half-cycles C_1 charges via R_3–D_1 and the upper half of R_4, and on negative half-cycles C_1 charges via R_3–D_2 and the lower half of R_4. R_4 thus enables the relative durations of the positive and negative slopes of the ramp waveform, and thus the mark/space ratio of the square wave, to be varied without appreciably affecting the operating frequency of the circuit. The operating frequency is independently variable via R_1.

XR-2206 multi-waveform circuits

The XR-2206 integrated circuit can readily be used as a multi-waveform generator. *Figure 4.6* shows how the i.c. can be connected to make a simple fixed-amplitude sine/triangle/square generator that uses a split power supply and covers the frequency range 10 Hz to 100 kHz in four decade ranges. The operating frequency of the circuit is determined by timing capacitor C_1 and timing resistors R_1–R_2. The timing capacitor must be a non-polarised type.

The sine/triangle mode of the circuit is selected via S_1, which does or does not connect R_4 between pins 13 and 14 of the i.c. With these

two pins open, a linear and symmetrical triangle wave is generated at output pin 2. With R_4 connected between pins 13 and 14, a sine wave is generated at output pin 2. The sine wave has a typical distortion content of 2 per cent when R_4 has the value shown. The distortion can be reduced to about 1 per cent by replacing R_4 with a 470 ohm variable resistor and adjusting for minimum distortion. The amplitudes of the sine and triangle waveforms can be adjusted or preset via R_3.

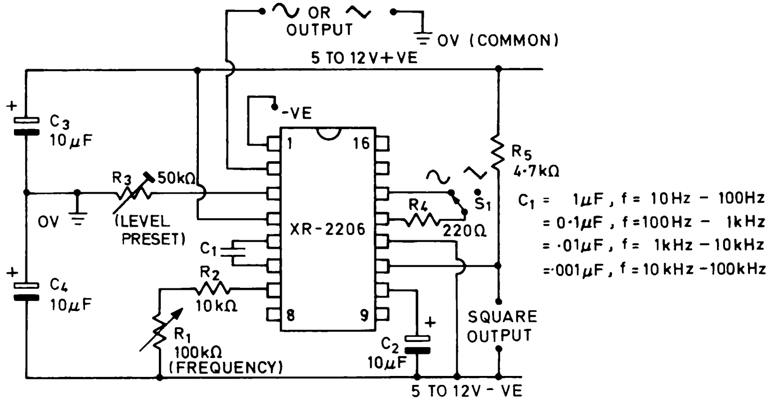


Fig. 4.6. Simple fixed-amplitude sine/triangle/square generator

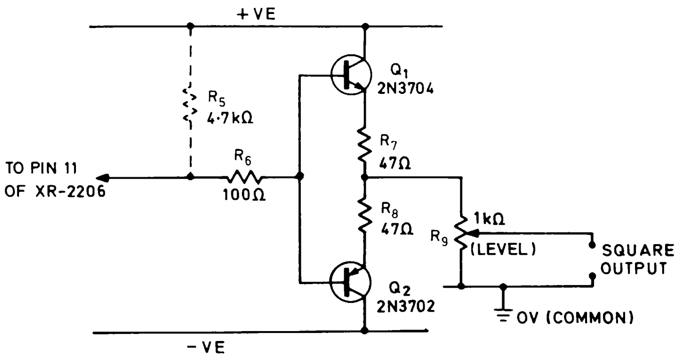


Fig. 4.7. Add-on circuit gives low-impedance, variable-amplitude access to square-wave output of XR-2206

A square-wave output is available at pin 11 of the i.c. simultaneously with the sine or triangle waveforms. This square wave is not suitable for directly driving low-impedance loads, and is intended only for driving high-impedance loads such as oscilloscope input or synchronisation terminals, etc. The rise and fall times of the square wave output signals are typically 250 ns and 50 ns respectively when pin 11 is loaded by 10 pF.

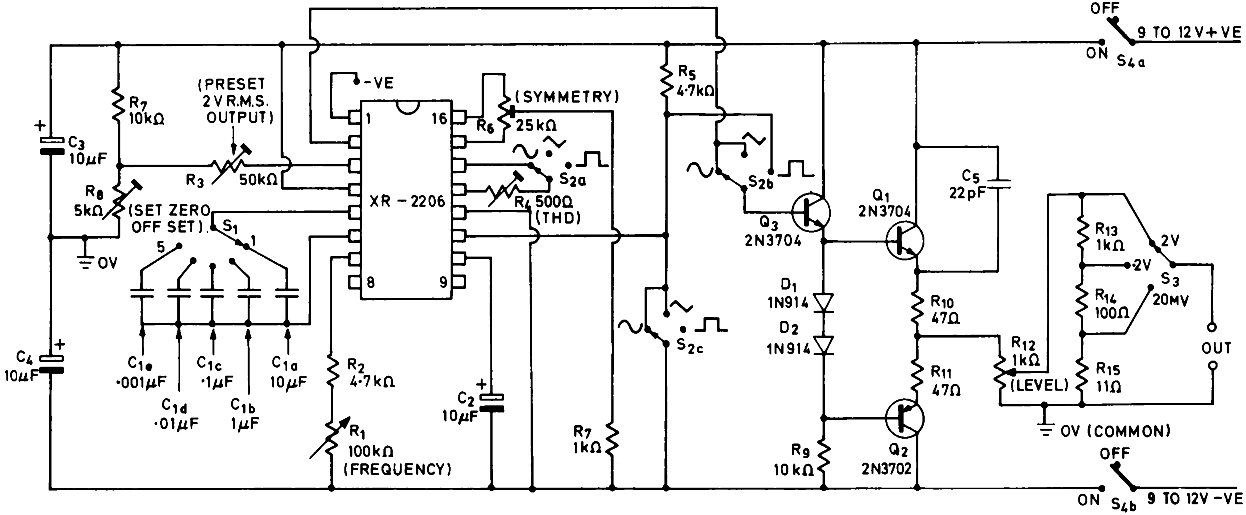
Figure 4.7 shows a simple add-on buffer stage that can be used to give low-impedance variable-amplitude access to the pin 11 square wave signal of the XR-2206. The circuit is a simple unbiased complementary emitter follower, which is driven directly from the pin 11 square-wave output of the i.c., and has short-circuit output protection via the 47 ohm resistors in series with the transistor emitters. The output level of the circuit is fully variable via R_9.

Figure 4.8 shows the circuit and performance data of a low-cost, high-performance sine/triangle/square generator that is designed around the XR-2206 i.c. The design is an improved version of the basic *Figure 4.6* circuit, and covers the frequency range 1 Hz to 200 kHz in five switched ranges. Frequencies are selected via range switch S_1 and 'fine frequency' control R_1. Each range of S_1 covers a full decade of frequency plus 100 per cent over-range at its upper frequency. The circuit incorporates t.h.d. adjustment of the sine wave (via R_4 and R_6), and gives a typical distortion factor of 0.5 per cent.

In this circuit the sine/triangle output of the i.c. is taken from pin 2, and all outputs are taken to a simple variable attenuator network via the Q_1–Q_2–Q_3 compound emitter-follower stage. R_8 enables the sine/triangle output to be centred on precisely zero volts, and R_3 enables the maximum sine-wave output to be set at 2 V r.m.s. The procedure for initially setting up the circuit when it is first built is as follows.

First set the attenuator controls to give maximum output, set the circuit to sine-wave mode at about 1 kHz, and then adjust R_8 to give zero offset of the output signal. This can be achieved by connecting a 0–2.5 V d.c. meter to the output of the circuit, and then adjusting R_8 for zero reading on the meter. Next, connect a 0–2.5 V a.c. meter to the output of the circuit, and adjust R_3 to give a sine-wave output of 2 V r.m.s. Finally, connect the sine-wave output to an oscilloscope or a distortion meter, adjust R_4 and R_6 to give minimum distortion of the sine wave, and recheck the d.c. offset and output amplitude. The setting up procedure is then complete, and the circuit is ready for use.

Figure 4.9 shows how the XR-2206 can be connected so that it generates a variable-slope ramp waveform or a pulse or rectangular waveform with a variable mark/space ratio. The output levels of both waveforms are fully variable via R_8. The action of the circuit is such that C_1 first changes linearly in one direction via R_1 until a certain 'switching' voltage is reached, at which point C_1 starts charging linearly in the reverse direction via R_2 until a second 'switching' voltage is reached, at which point the action repeats and C_1 starts charging via R_1 again. Each time the circuit reaches a 'switching' level, the pin 11 output switches abruptly from a positive to a negative level, or vice versa.



Waveform stability (typ.)
0.002% per °C
0.01%/V supply sensitivity

S_1 *ranges*

Position 1:	1Hz-20Hz
2:	10Hz-200Hz
3:	100Hz-2kHz
4:	1kHz-20kHz
5:	10kHz-200kHz

Output waveforms

Sine: distortion (typ.)	= 0.5%
Triangle: linearity (typ.)	= 1%
Square: rise time (typ.)	= 200ns
fall time (typ.)	= 100ns

S_1 = Single-pole 5-way switch
S_2 = Three-pole 3-way switch
S_3 = Single-pole 3-way switch
S_4 = Two-pole 2-way switch

Max. output levels
(with 9-0-9 V supply)

Sine	= 5.6 V pk-pk
Triangle	= 12 V pk-pk
Square	= 16 V pk-pk

Total current consumption (typ.) = 20 mA

Note: All capacitors are non-polarised types.

Fig. 4.8. Circuit and data of low-cost, high-performance 1 Hz to 200 kHz sine/triangle/square generator

Thus the rising and falling slopes of the ramp waveform, and the 'on' and 'off' times of the rectangle or pulse waveform, can be independently controlled via R_1 and R_2. The operating frequency of the circuit is given as:

$$f = \frac{2}{C_1}\left(\frac{1}{R_1 + R_2}\right)$$

The ramp output waveform of the *Figure 4.9* circuit is taken to 'level' control R_8 directly from pin 2 of the i.c., and the pulse waveform is

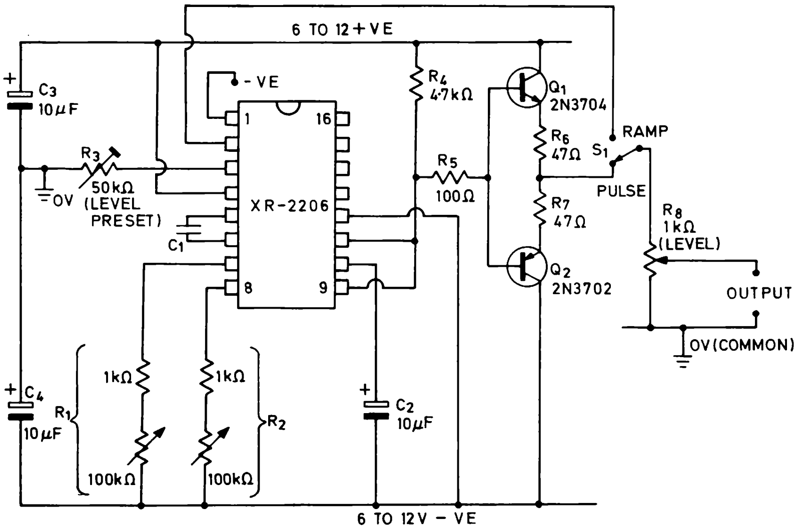


Fig. 4.9. Variable pulse and ramp generator circuit

taken to R_8 from pin 11 via the Q_1–Q_2 emitter-follower stage. Both output waveforms of the circuit swing symmetrically about the zero-volts level. The versatility of this circuit can be increased, if desired, by replacing the existing pulse output stage with that shown in *Figure 4.10*. This circuit enables positive, negative or symmetrical output pulses to be selected via S_2.

Here, load resistor R_4 is replaced with a pair of 2.7 kΩ 5 per cent resistors. With two-pole switch S_2 in position 1 the pulse output of the circuit is effectively taken from the junction of these two resistors, so the output switches between the fully positive and half-supply or 'ground' volt levels, and the circuit thus gives positive output pulses. In position 2 of S_2 the output is effectively taken from pin 11 of the i.c., so

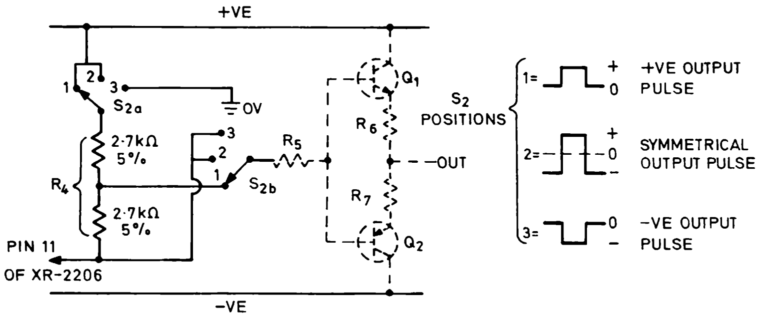


Fig. 4.10. Alternative output stage gives positive, negative or symmetrical pulses from the Fig. 4.9 circuit

symmetrical output pulses are available. In position 3 of S_2 the output is again taken from pin 11 of the i.c., but the top end of R_4 is connected to the zero-volts line, so the output switches between the zero and negative voltage rails, and negative output pulses are available from the circuit.

U.J.T. multi-waveform generator circuits

Unijunction transistors can readily be used to generate both sawtooth and pulse or rectangular waveforms. *Figure 4.11* shows the practical

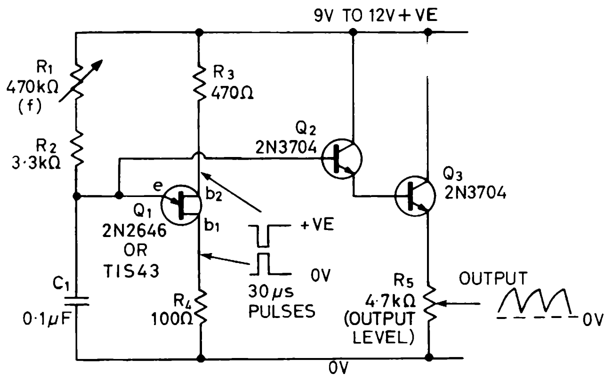


Fig. 4.11. U.J.T. circuit generates pulse and non-linear sawtooth waveforms; frequency range 25 Hz to 3 kHz

circuit of a basic free-running u.j.t. oscillator, which covers the frequency range 25 Hz to 3 kHz and produces a non-linear sawtooth across R_5 and a 30 μs positive pulse across R_4 and a 30 μs negative pulse

across R_3. The waveform period is determined by the values of R_1–R_2 and C_1, and the pulse widths are determined by the values of C_1 and R_4. This circuit can be made to produce a linear sawtooth waveform by replacing the R_1–R_2 resistor charging network with a constant-current generator circuit, as shown by R_1–R_2–R_3–R_4–D_1–Q_1 in *Figure 3.2.*

Figure 4.12 shows how a free-running u.j.t. oscillator can be used in conjunction with a 741 operational amplifier to make a circuit that

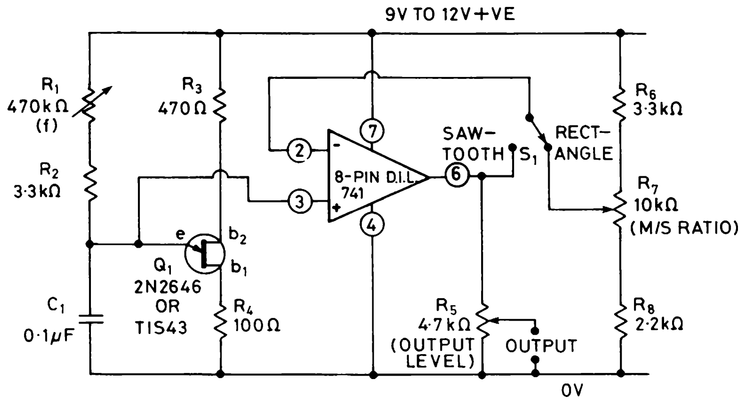


Fig. 4.12. 25 Hz to 3 kHz generator produces a non-linear sawtooth, or a rectangle waveform with infinitely variable M/S ratio

can produce a non-linear sawtooth waveform or a rectangular waveform with an infinitely variable mark/space ratio. Here, when S_1 is put into the 'sawtooth' position the op-amp is connected as a unity-gain voltage-follower circuit, with its input fed from timing capacitor C_1 of the u.j.t. oscillator circuit. Consequently a variable-amplitude sawtooth waveform is available across 'output level' control R_5 under this condition.

When S_1 is put into the 'rectangle' position the op-amp is connected as a simple voltage comparator switch, with its non-inverting input fed from C_1 and its inverting input fed from variable potential divider R_6–R_7–R_8, which is connected across the supply lines of the circuit. The action of this comparator is such that its output switches rapidly from positive to negative saturation, or vice versa, as the instantaneous sawtooth voltage passes through the voltage level set on the slider of R_7. Consequently a rectangular waveform of sawtooth frequency is available across R_5 under this condition, and has a mark/space ratio that is infinitely variable (from 0 : 1 to 1 : 0) via R_7.

The *Figure 4.12* circuit can be modified so that it generates a linear sawtooth waveform by simply using a constant-current generator to

charge timing capacitor C_1, as shown in the circuit of *Figure 4.13*. This circuit covers the frequency range 60 Hz to 7 kHz in two decade ranges.

The *Figure 4.12 and 4.13* circuits provide useful rectangular waveforms

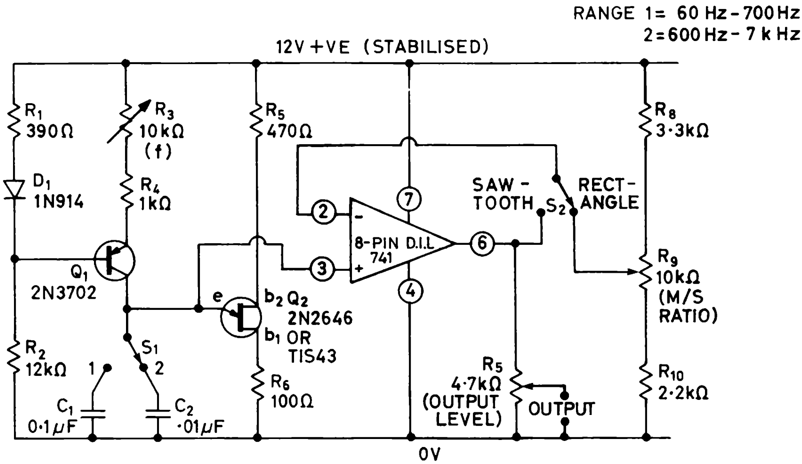


Fig. 4.13. 60 Hz to 7 kHz generator produces a linear sawtooth, or a variable M/S ratio rectangle

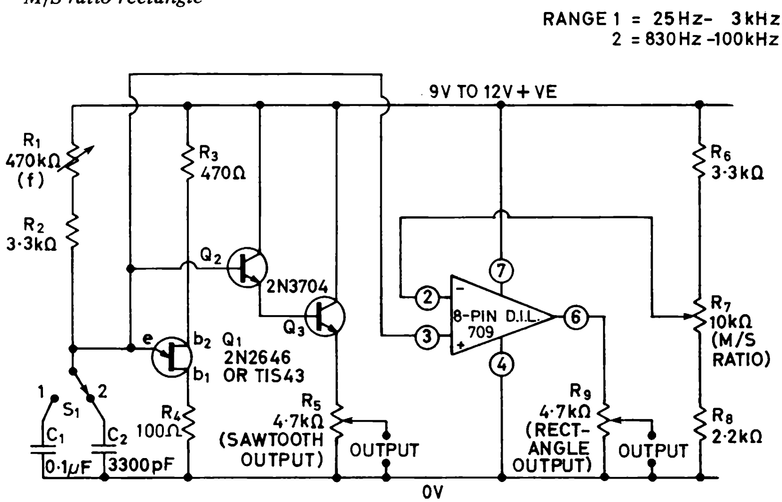


Fig. 4.14. 25 Hz to 100 kHz sawtooth/rectangle generator

up to maximum frequencies of about 10 kHz. Operation beyond this range is poor, because of the slew rate limitations of the 741 operational amplifier. *Figure 4.14* shows how the *Figure 4.12* circuit can be modified

so that it provides useful non-linear sawtooth and sharp rectangular waveforms up to maximum frequencies of about 100 kHz. The circuit covers the frequency range 25 Hz to 100 kHz in two overlapping ranges.

The circuit has two independent outputs. The sawtooth output is available across R_5, and is taken from the main timing capacitor via the Q_2-Q_3 Darlington emitter-follower stage. The variable mark/space ratio rectangular waveform is available across R_9, and is taken from the output of a 709 operational amplifier that is wired as a simple voltage comparator stage. This op-amp has a reasonably fast slew rate, and provides the rectangular output waveform with typical rise and fall times of 1.5 μs and 0.5 μs respectively.

Type 555 triggered pulse/sawtooth generator

To complete this chapter, *Figure 4.15* shows how a type 555 timer i.c. can be connected so that it acts as a triggered generator that provides both a linear sawtooth output (across R_6) and a positive pulse output

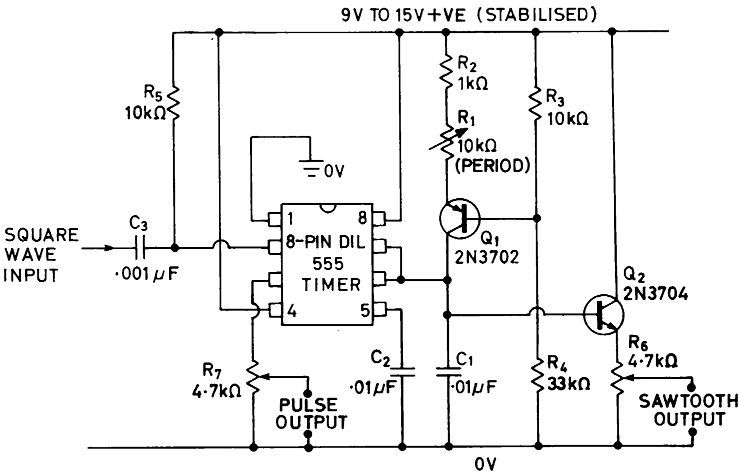


Fig. 4.15. Triggered 55 μs to 600 μs pulse and sawtooth generator

(across R_7). The sawtooth and pulse waveforms have identical timing periods, which cover the range 55 μs to 600 μs with the component values shown when a 9 V supply is used. The period range can be changed by using alternative C_1 values. The period is directly proportional to the C_1 value.

Note that this circuit is a simple modification of the *Figure 3.8* circuit, and a more complete description of its operation is given in Chapter 3.

CHAPTER 5

SPECIAL WAVEFORM GENERATORS

In addition to the sine, square, triangle, ramp and pulse waveform generators discussed in previous chapters, a variety of other 'special' waveform generators are often encountered or required in electronics. Examples of these are 'white noise' generators, staircase waveform generators, crystal-controlled generators, waveform synthesisers, and special-effect 'sound' generators for use in electronic alarm systems, etc. This chapter shows a variety of these 'special' waveform-generator circuits.

Modifying existing waveforms

It has been shown in earlier chapters that existing waveforms can often be changed into alternative forms by passing them through simple converter circuits. Sine, triangle and ramp waveforms can, for example, be changed into square or rectangle form by passing them through a level-sensitive switch such as a Schmitt trigger, and triangle waveforms can be converted into sine waves by feeding them through a suitable diode shaping matrix, etc. *Figures 5.1 to 5.5* show a variety of ways of modifying existing waveforms by passing them through simple *C–R* differentiating and diode clamping or clipping networks.

Looking first at *Figure 5.1*, this shows how the shape and level of a symmetrical or non-symmetrical square wave can be changed by passing it through a simple *C–R* differentiating network with a selected time constant. In the examples shown in the diagram the input waveform has a total period of 1 ms (= 1 kHz), and the *C–R* network gives time constants of (a) 100 ms, (b) 1 ms, or (c) 0.01 ms.

In the *Figure 5.1a* circuit, in which the *C–R* time constant is long relative to the period of the input waveform, the shape and dimensions of the output waveform are identical to the input, but are shifted in level so that the output waveform swings about the zero-volts value. Note that the –ve peak/+ve peak ratio of the output is directly proportional to the mark/space ratio of the input signal.

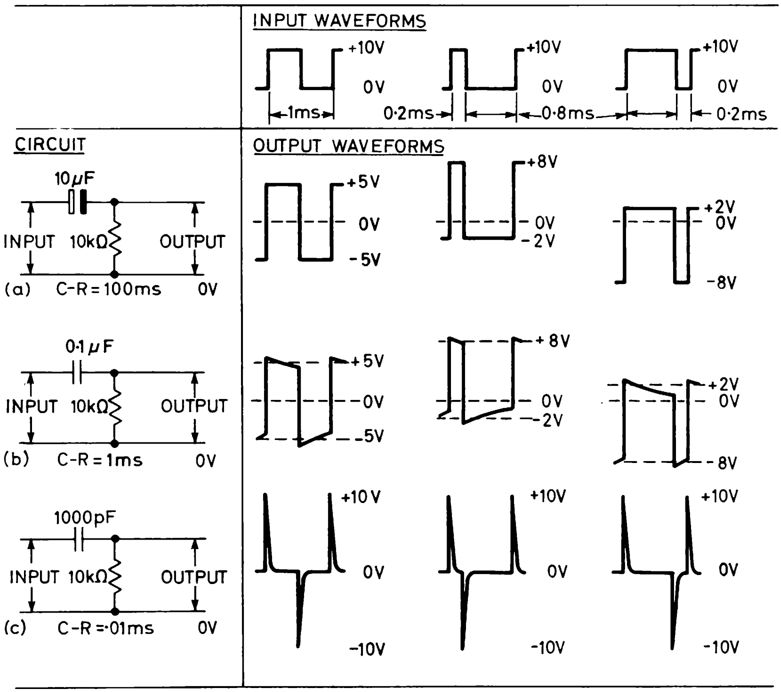


Fig. 5.1. Effects of C–R time constants on symmetrical and non-symmetrical square-wave signals

In the *Figure 5.1b* circuit, in which the *C–R* time constant is equal to the time constant of the input signal, the output level is again shifted to around the zero-volts level, but in this case the waveform is modified as well. Note in this circuit that the peak-to-peak amplitude of the output signal is greater than the peak-to-peak amplitude of the input signal.

In the *Figure 5.1c* circuit, in which the *C–R* time constant is very short relative to that of the input signal, the output level is shifted so that the signal swings symmetrically about the zero-volts value, irrespective of the input signal's mark/space ratio. The output differs greatly from

the input, and takes the form of two spike or pulse waveforms (one positive, the other negative) per input cycle. Note that the peak-to-peak amplitude of the output signal is double that of the input signal.

Figure 5.2 shows what happens to the output waveforms of the *Figure 5.1* circuit when a positive clamping or discriminating diode is wired across the output of the *C–R* differentiating network. The major

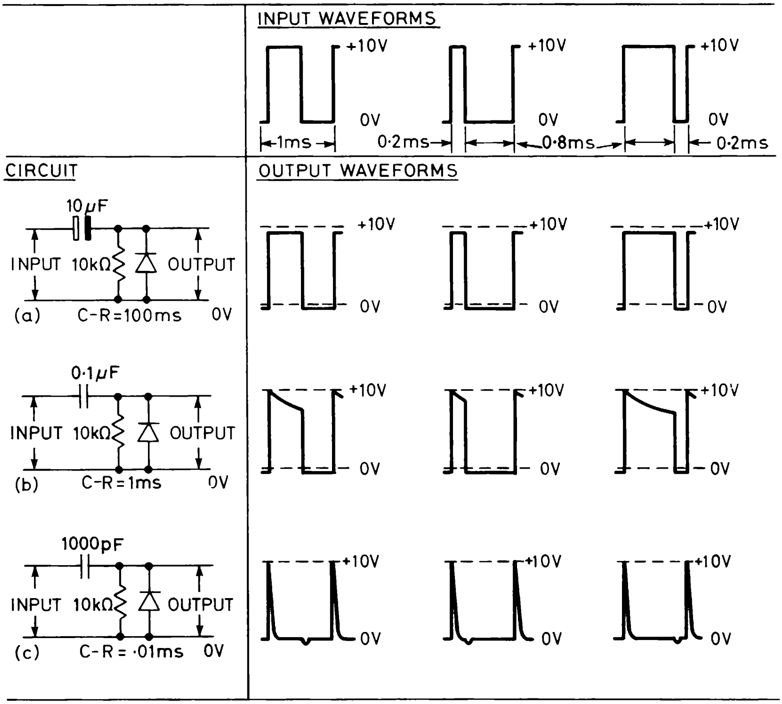


Fig. 5.2. Effects of C–R time constants plus positive clamping diode on symmetrical and non-symmetrical square-wave signals

effect of the diode is simply to clamp the bottom of the output signal to the zero-volts line, so that only positive output signals are obtained. Note in the *Figure 5.2c* circuit that the negative output signal spike is virtually eliminated, so that only a single positive output spike is obtained from each input cycle.

Figure 5.3 shows the effect of changing the polarity of the clamping or discriminating diode of the *Figure 5.2* circuit. In this case the tops of the output signals are clamped to the zero-volts line, and only negative output signals are obtained from the circuit.

Figure 5.4 shows how symmetrical sine or square waveforms can be modified by passing them through a long-time-constant differentiating network combined with different diode configurations. The *C–R* network has a time constant of 100 ms, compared to the input signal period of 1 ms.

The *Figure 5.4a* circuit consists of a *C–R* network only, and simply causes the signal to shift level so that it swings symmetrically about the zero-volts value.

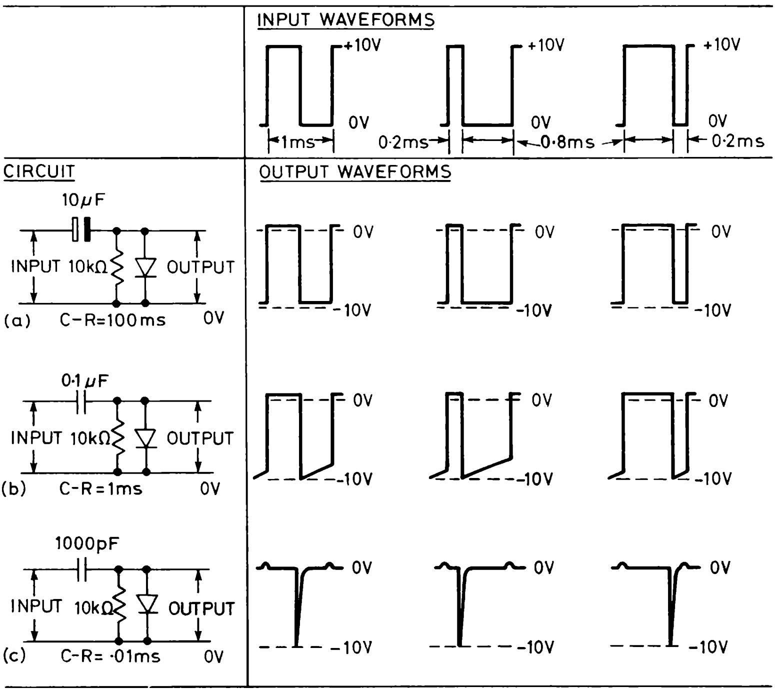


Fig. 5.3. Effects of C–R time constants plus negative clamping diode on symmetrical and non-symmetrical square-wave signals

The *Figure 5.4b* circuit has a positive clamping diode wired across its output. The effect of this diode is to clamp the bottom of the waveform to the zero-volts line, and give positive output signals only. In the case of the square wave, the signal is simply level-shifted, so that the output signal amplitude is roughly equal to that of the input signal. In the case of the sine wave, on the other hand, the bottom half of the waveform is virtually chopped off, and the output waveform is highly distorted.

The *Figure 5.4c* circuit has a negative clamping diode wired across its

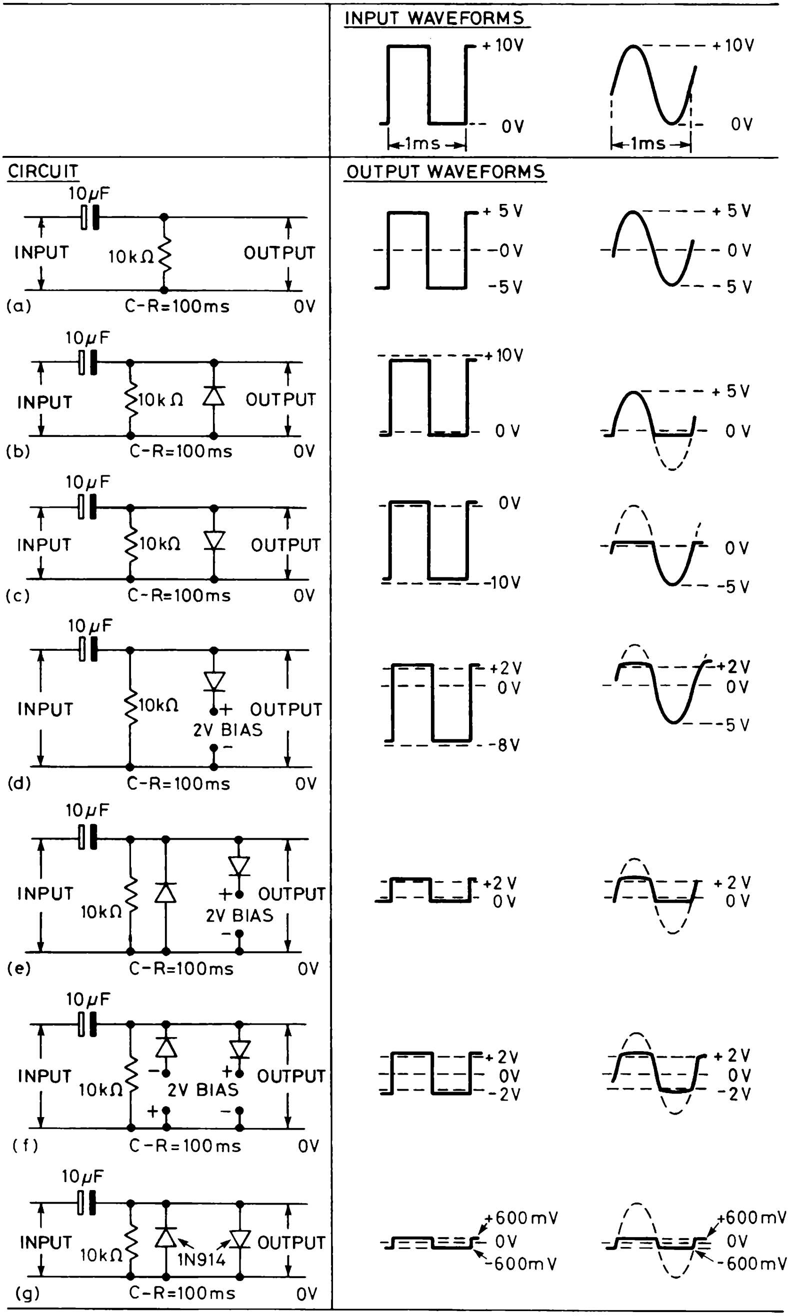


Fig. 5.4. Effects of long-time-constant C–R network plus clamping and/or clipping diodes on symmetrical sine- and square-wave signals

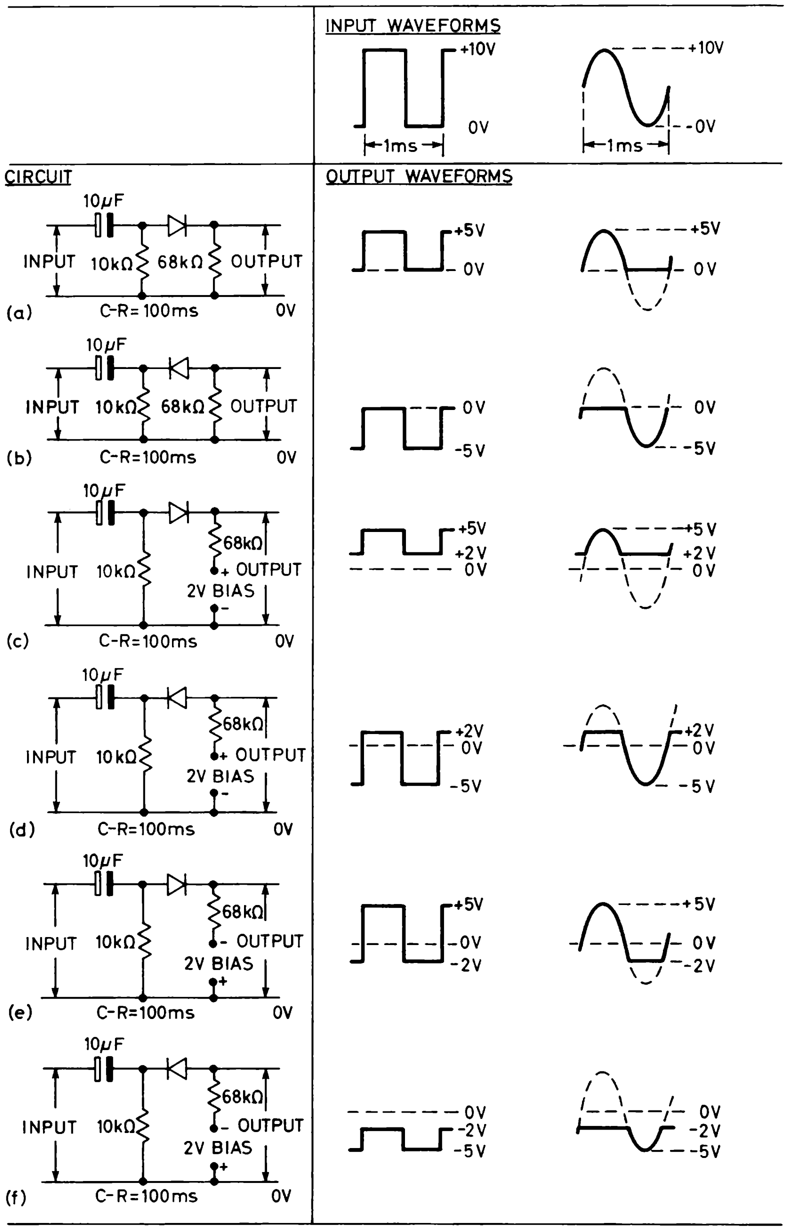


Fig. 5.5. Effects of long-time-constant C–R network plus series output diode on symmetrical sine- and square-wave signals

output. This diode gives an effect that is the reverse of that of the *Figure 5.4b* circuit, and gives negative output signals only.

The *Figure 5.4d* circuit has a positively biased 'negative' diode across its output. The diode is biased at +2 V in the example shown, and its effect is to clamp the top of the waveform to the +2 V reference level. When the square wave is fed through this circuit its mean levels are shifted, so that its output switches between +2 V and –8 V. When the sine wave is fed through the circuit its lower half is unaltered, but its top half is clipped at +2 V. The reverse effect can be obtained by simply changing the polarity of the diode.

Figure 5.4e shows the effect of combining the 'clamping' diode of the *Figure 5.4b* circuit with the 'clipping' diode of the *Figure 5.4d* circuit. This circuit causes the lower half of the output waveform to be clamped to just below zero volts and the top half to be clipped at +2 V. Note that the output 'sine' wave is greatly distorted.

Figure 5.4f shows the effect of combining the positively biased 'negative' diode of *Figure 5.4d* with a negatively biased 'positive' diode. Each diode is biased at 2 V in the examples shown. This circuit causes the output signals to swing symmetrically about the zero-volts reference value, but to be clipped at +2 V and –2 V.

Figure 5.4g shows the effect of wiring both 'positive' and 'negative' silicon clamping diodes across the output of the *C–R* network. This circuit can be regarded as either a combination of the *Figure 5.4b and c* circuits, or as equal to the *Figure 5.4f* circuit with zero-volts bias applied to each diode. The effect of the circuit is to cause the output signal to swing symmetrically about the zero-volts reference value, but to be clipped at the silicon diode conduction values of about +600 mV and –600 mV.

Finally, *Figure 5.5* shows the effects of placing simple 'rectifier' diodes in series with the outputs of the *C–R* networks. In each case the *C–R* network simply causes the diode input signals to swing symmetrically about the zero-volts level, and the diode rectifies or cuts off part of the output signal. The *Figure 5.5a* circuit cuts off the whole bottom half of the signal and gives a positive output, and the *Figure 5.5b* circuit cuts off the whole of the top half of the signal and gives a negative output.

In the *Figure 5.5c and d* circuits a bias voltage is effectively applied to the series diodes, and controls the point at which diode conduction can start. Bias values of +2 V are used in the examples shown. The action of the *Figure 5.5c* circuit is such that all signals below the +2 V reference level are eliminated, so only those parts of the signal with peak values in excess of +2 V appear at the output. The action of the *Figure 5.5d* circuit is such that all signals above the +2 V reference level

are eliminated, so only those parts of the signal with values below the +2 V level appear at the output. Alternative 'clipper' action can be obtained by applying negative bias voltages to the diodes of the *Figure 5.5c and d* circuits, as shown in *Figures 5.5e and f*. The clipping levels of these four circuits can be changed by using alternative bias-voltage values.

It should be noted that all waveforms shown in the *Figure 5.2 to 5.5* circuits are approximate only, and do not necessarily take account of the effects of diode volt drops or the effects of input signal-source impedances.

It should also be noted that a wide variety of potentially useful waveforms can be obtained from the *Figure 5.1 to 5.5* circuits by feeding them with triangle, ramp or sawtooth input voltages, or by feeding the outputs of these circuits to simple filter networks.

White noise generator

White noise can be simply described as a signal containing a full spectrum of randomly generated frequencies that have equal mean power when averaged over a unit of time. White noise is of value in testing a.f. and r.f. amplifiers, and is widely used in 'science fiction' sound-effects generator systems. Zener diodes act as excellent sources of white noise.

Figure 5.6 shows the practical circuit of a simple but useful white-noise generator. Here, resistor R_2 and the zener diode are wired as a

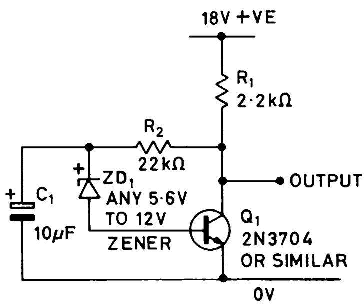


Fig. 5.6. White-noise generator

negative-feedback loop between the collector and base of transistor Q_1, and thus stabilise the d.c. working levels of the circuit. The feedback loop is decoupled via C_1. Consequently the zener diode acts as a noise source that is wired in series with the base of the transistor, which

amplifies the zener-diode noise to a useful level. Any 5.6 V to 12 V zener diode can be used in the circuit, which typically gives a mean noise output of one volt peak-to-peak.

Wide-range crystal oscillator

Quartz crystals have very sharply defined resonant frequencies, and are consequently widely used as highly stable frequency standards. *Figure 5.7* shows the practical circuit of a wide-range crystal oscillator that can be used with virtually any crystals having resonant frequencies in the approximate range 50 kHz to 10 MHz.

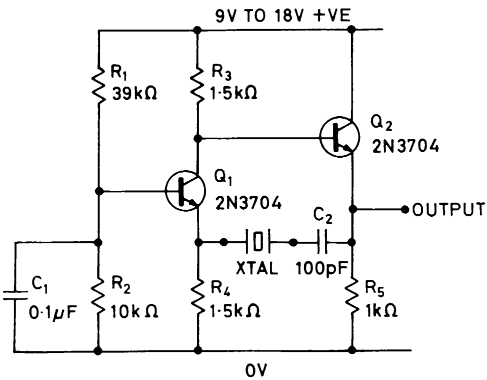


Fig. 5.7. Wide-range crystal oscillator can be used with virtually any 50 kHz to 10 MHz crystal

The operation of the *Figure 5.7* circuit is quite simple. Transistor Q_1 is wired as a common-base amplifier, with its base biased by R_1 and R_2 and decoupled by C_1, and with its input signal applied to its emitter and its output taken from its collector. Note that the input and output signals of this common-base stage are in phase, and that voltage gain occurs between input and output. Transistor Q_2 is wired as a simple emitter-follower stage, with its input taken from the collector of Q_1 and its output appearing across R_5. Note that the input and output signals of this emitter-follower stage are in phase, and that unity voltage gain occurs between input and output.

Thus substantial voltage gain occurs between the input of Q_1 and the output of Q_2, and the Q_1 input and Q_2 output signals are in phase. Consequently this circuit oscillates when a tuned circuit (such as a quartz crystal) that presents a low impedance and zero phase shift at its resonant frequency is connected between the emitters of Q_1 and

Q_2. As already mentioned, the circuit can be used with virtually any crystals having resonant frequencies in the range 50 kHz to 10 MHz. The circuit gives output signals of several volts peak-to-peak amplitude. The high-frequency performance of the circuit can be improved by wiring a small inductor, with a value of a few tens of microhenries, in series with the R_3 collector load of Q_1.

Staircase waveform-generator circuits

Staircase generator circuits are provided with input and output terminals, and the circuit action is such that, with the output signal starting at a low level, the output level rises by a discrete step each time the input signal is applied, until eventually, after a predetermined number of input cycles, the output waveform switches abruptly back to the low level and the whole sequence repeats itself. The output signal thus takes the form of a 'staircase' with a predetermined number of steps.

Staircase generators can thus be used as pulse counters, frequency dividers or step-voltage generators for use in transistor curve tracers, etc.

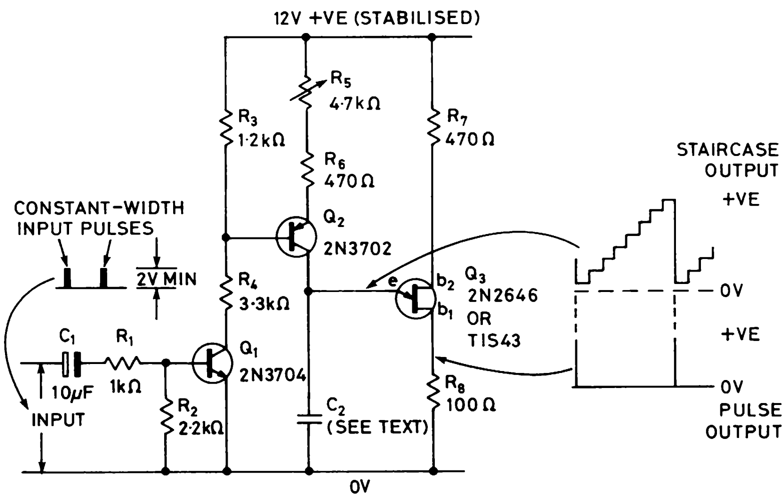


Fig. 5.8. Linear staircase-generator circuit

Figure 5.8 shows the practical circuit of a 'linear' staircase generator. Here, Q_1 is wired as a simple common-emitter amplifier, which controls constant-current generator Q_2, which controls the charging current of timing capacitor C_2, which is coupled to the input of unijunction

transistor Q_3. Normally, in the absence of an input signal, Q_1 and Q_2 are cut off, and no charge is fed into C_2. When a constant-width positive input pulse is fed to the circuit via C_1, Q_1 and Q_2 are driven on and charge current is fed into C_2, which charges linearly for the (fixed) duration of the pulse. The C_2 voltage thus increases by a fixed amount each time an input pulse is applied.

In the absence of a pulse, there is no discharge path for C_2, so the voltage stays on this capacitor. Successive input pulses each increase the C_2 charge voltage by a fixed amount, until, after a predetermined number of pulses, the C_2 voltage reaches the trigger potential of Q_3, at which point the u.j.t. fires and discharges C_2, thus restarting the operating cycle.

If the input pulses to the circuit are applied at a constant repetition frequency, the signal across C_2 is a linear staircase waveform, and a brief output pulse is available across R_8 each time the u.j.t. fires. If the input frequency is not constant, the staircase is non-linear, but the R_8 pulse again appears after a predetermined number of input pulses have been applied. Stable count or division ratios or staircase steps from two up to about twenty can be obtained.

It is important to note that this circuit must be fed with constant-width input pulses if stable operation is to be obtained, and that the width of these pulses must be small relative to the pulse repetition period. The value of C_2 is determined by these considerations, and is best found by trial and error. Once a C_2 value has been selected, the division ratio can be varied over a range of about 10 : 1 via R_5. Many of the triggered pulse-generator circuits described in Chapter 2 can be used to provide the input pulses to this circuit.

It should also be noted that the staircase output waveform appearing across C_2 is at a high impedance level. This waveform can be converted to a low impedance level by interposing a Darlington emitter-follower stage between C_2 and the final output terminals of the circuit.

An alternative staircase-generator circuit is shown in *Figure 5.9*. This circuit, which is sometimes known as a 'diode pump counter', also acts as a frequency divider or counter, but gives a non-linear staircase output. It has the advantage, however, that counting (and thus the number of staircase steps) is almost independent of the shape of the input waveform.

Here, with no input applied, Q_1 is cut off, and timing capacitor C_3 charges via R_3–C_2 and D_1. C_2 and C_3 act as a capacitive potential divider, so a fixed fraction of the supply voltage appears across C_3. When an input pulse is applied, Q_1 is driven to saturation and C_2 is discharged via Q_1 and D_2, but C_3 is prevented from discharging by D_1. When the input pulse is removed again, C_2 again charges via D_1 and R_3, and places another fraction of the supply voltage on C_3. Thus at the end of each

input pulse the C_3 voltage increases by a fixed step, until eventually the u.j.t. fires and discharges C_3, and the count cycle starts over again. The actual input pulse shape has very little effect on circuit operation.

The division ratio of the circuit is roughly equal to $C_2/(C_2 + C_3)$. The ratio is, however, affected by a number of variable factors, including operating frequency, so the values of C_2 and C_3 are best found by trial

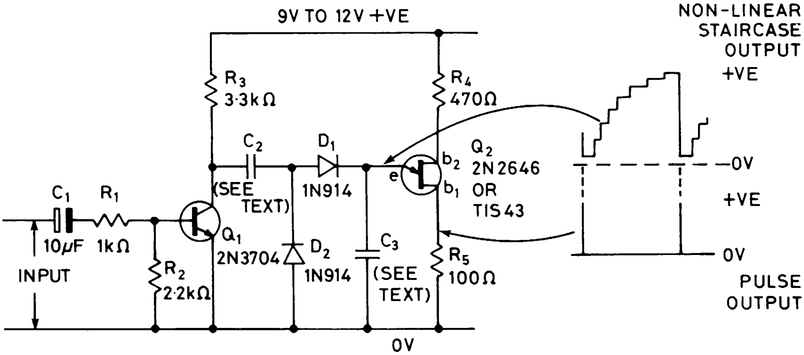


Fig. 5.9. Non-linear staircase-generator or diode pump counter

and error. Once component values have been selected, the circuit will give stable division over quite a wide range of input-frequency variation. Stable division ratios up to 10 : 1 can be easily obtained.

Note that the non-linear output waveform appearing across C_3 is at a high impedance level. It can be converted to a low impedance by interposing a Darlington emitter-follower buffer stage between C_3 and the final output terminals of the circuit.

Digital sine-wave synthesiser

A sine wave can be created digitally by first building up the rough outline of a sine wave in a number of digital steps, and then removing the high frequency components of the digital signals via a simple filter network. The basic technique is illustrated in *Figure 5.10*.

Here, a 'clock' signal is fed to the input of a five-stage walking ring or Johnson counter; four of the outputs of the counter are added together, via a simple resistor weighing network, to produce a crude sine wave, which is then converted into a reasonably pure form via low-pass capacitor C_1. The frequency of the sine-wave output signal is one-tenth that of the basic clock signal. Consequently the lowest harmonic signals of any consequence to the final sine-wave signal are the ninth, eleventh, nineteenth, twenty-first, and so on, and these signals can easily be removed

by the simple filter network. Note that, since the sine wave is generated digitally, it contains no significant even harmonics. Also note that the greater the number of digital steps used to generate the basic sine wave, the easier it is to eliminate unwanted harmonic signals.

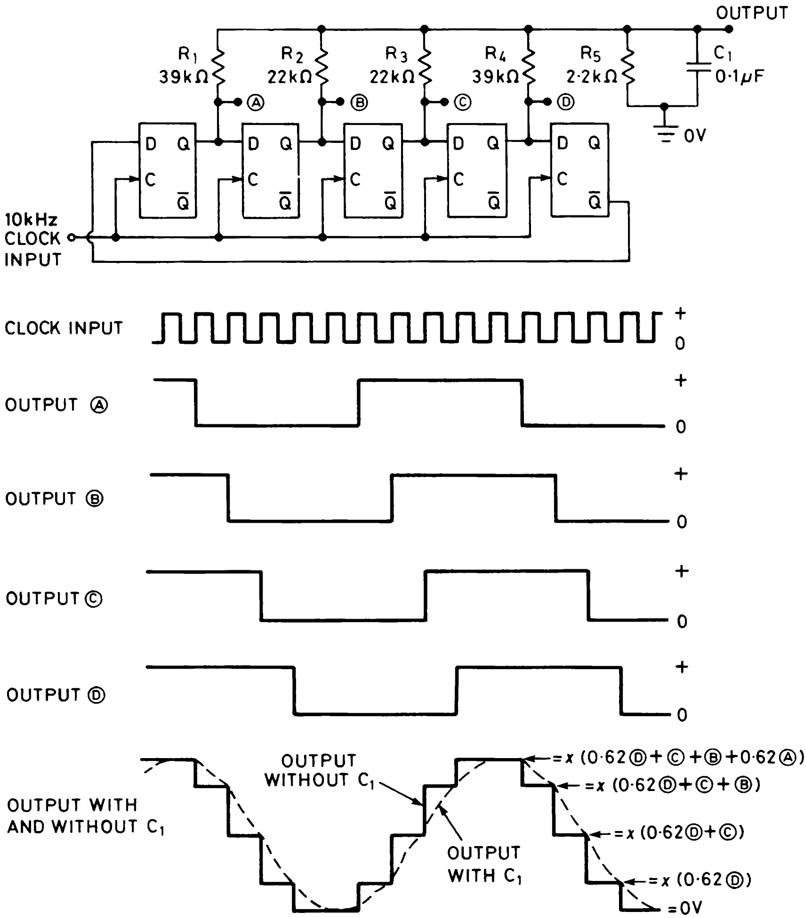
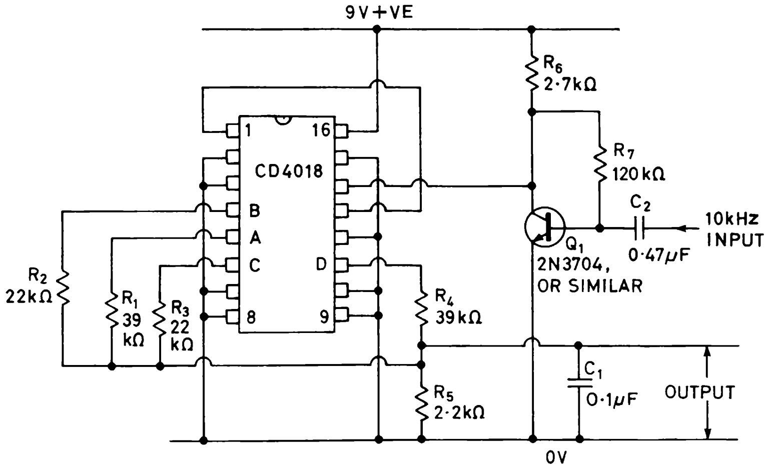


Fig. 5.10. Basic circuit and waveforms of 1 kHz digital sine-wave synthesiser

Figure 5.11 shows the practical circuit of a 1 kHz digital sine-wave synthesiser of the type described above. The circuit is built around a CD4018 COS/MOS presettable divide-by-N counter. Transistor Q_1 is used to convert an external 10 kHz input signal into a form suitable for



Harmonic	*Frequency*	*Amplitude* (dB) Without C_1 (ref. 0.66 V r.m.s.)	With C_1 (ref. 0.42 V r.m.s.)
1	1 kHz	0	0
3	3 kHz	–44	–51
5	5 kHz	–65	<–70
7	7 kHz	–50	<–70
9	9 kHz	–19	–36
11	11 kHz	–20.5	–40
13	13 kHz	–58	<–70
15	15 kHz	<–70	<–70
17	17 kHz	–57	<–70
19	19 kHz	–25	–49
21	21 kHz	–27	–51
23	23 kHz	–64	<–70
25	25 kHz	<–70	<–70
27	27 kHz	–63	<–70
29	29 kHz	–30	–57
31	31 kHz	–30	–58
33	33 kHz	<–70	<–70

Note. When the basic output of the circuit is fed through a second-order filter, all harmonics are greater than 65 dB down on the fundamental

Fig. 5.11. Practical circuit and measured performance details of 1 kHz digital sine-wave synthesiser

clocking the i.c. The measured performance of this circuit, both with and without filter capacitor C_1, is tabulated in the diagram.

Note that with C_1 in place the lowest significant harmonic of the 1 kHz sine wave is the ninth, at –36 dB relative to the fundamental. The sine wave thus has a total harmonic distortion content of about 2 per cent. If a second-order low-pass filter is used in place of C_1 in this circuit, all harmonics are reduced to better than 65 dB down on the fundamental, corresponding to a total harmonic distortion content of about 0.1 per cent. The *Figure 5.11* circuit thus provides a simple and inexpensive means of generating good-quality sine waves that are of fixed frequency or are variable over a narrow frequency range.

Alarm-call sound generator circuits

The outputs of most low-frequency waveform generators can be fed to loudspeaker systems via simple power-amplifier stages and used to produce alarm-call sounds for use in conjunction with electronic alarm sensing circuits. The alarm-call sounds generated can take a wide variety of forms: they may be continuous or pulsed sounds, warble tones, or variable sounds such as those associated with the 'Kojak' police car sirens or the Star Trek 'Red Alert' alarms. A variety of alarm-call generator circuits are presented in the remainder of this chapter.

Two types of integrated circuit have particular appeal for use in alarm-call generator systems. The first of these is the CD4001 COS/MOS quad 2-input NOR gate. The attractions of this i.c. in such applications are that the four available gates of the device can easily be interconnected in a variety of basic waveform-generator configurations, that the i.c. draws negligible quiescent current when it is in the 'standby' state, and that the i.c. can be used with any d.c. supply in the range 3 V to 15 V. *Figures 5.12 to 5.20* show a variety of alarm-call generator circuits that are designed around the CD4001 i.c.

Figure 5.12 shows the circuit of a low-power monotone (800 Hz) alarm-call generator. Here, only half the i.c. is used, connected as a gated 800 Hz astable multivibrator, with its output feeding to a small speaker via buffer transistor Q_1. The configuration is such that Q_1 is biased fully off when the i.c. is disabled, so the circuit draws a typical standby current of only 1 μA or so. The alarm can be gated on by driving pin 1 of the i.c. to the logic 0 of ground level. This alarm can thus be turned on electronically by applying a suitable signal to pin 1 of the i.c., or it can be gated manually via a switch connected between pin 1 and the ground

or positive supply lines, as shown in *Figures 5.12a and b* respectively.

The *Figure 5.12* circuit (and also the circuits of *Figures 5.13 to 5.16*) is intended for low-power applications only, and can be used with any speaker impedance in the range 3 Ω to 100 Ω, and with any supply in the range 5 V to 15 V. Note that resistor R_x must be wired in series with the speaker, and must be chosen so that the total series resistance

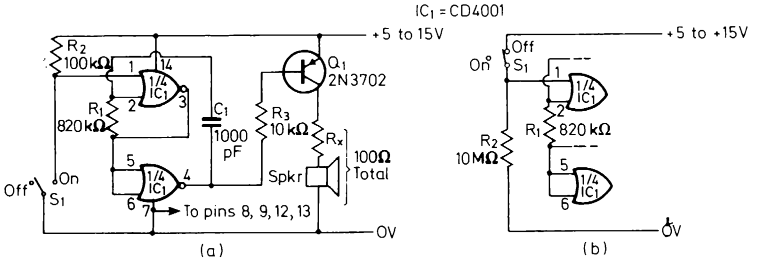


Fig. 5.12. Low-power monotone (800 Hz) alarm-call generator; (a) close-to-operate; (b) modification for break-to-operate

of R_x and the speaker approximates 100 Ω, to keep the dissipation of Q_1 within acceptable limits. The actual power-output level of the circuit depends on the values of speaker impedance and supply voltage that are used, but is only of the order of milliwatts. It is shown later in this section that the power output levels of these generators can easily be boosted to as high as 18 W.

The basic alarm-generator circuit of *Figure 5.12* can be redesigned to give a variety of types of generator function. *Figure 5.13* shows how the two 'spare' gates of the i.c. can be utilised to give a pulsed-tone type of operation. Here, the two right-hand gates of the i.c. are wired as a gated 800 Hz astable generator, as already described, and the two left-hand gates are wired as a low-frequency (6 Hz) gated astable, which is gated via S_1 (or an external logic 0 signal) and in turn gates the 800 Hz generator on and off.

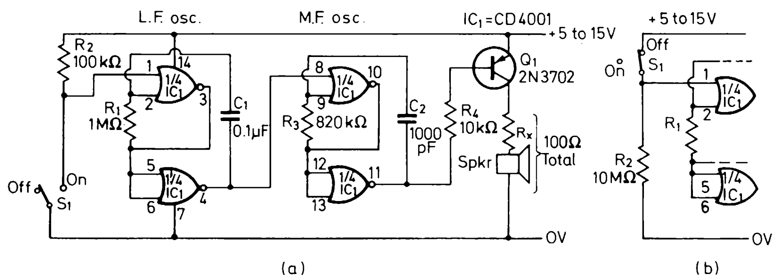


Fig. 5.13. Pulsed-tone alarm-call generator: (a) close-to-operate; (b) modification for break-to-operate

Figure 5.14 shows how the *Figure 5.13* circuit can be modified so that it produces a warble-tone alarm signal. These two circuits are basically similar, but in the latter case the 6 Hz astable is used to modulate the frequency of the right-hand astable rather than to pulse

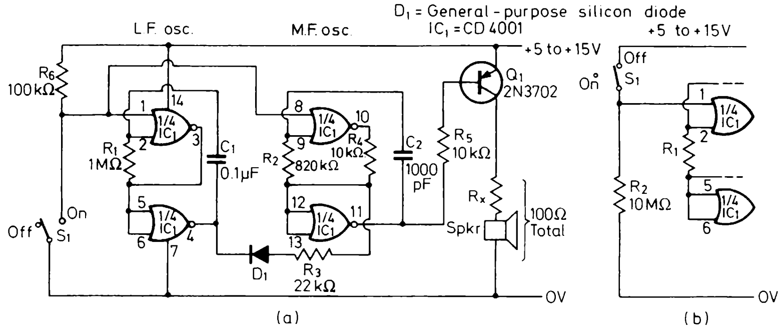


Fig. 5.14. Warble-tone alarm-call generator: (a) close-to-operate; (b) modification for break-to-operate

it on and off. Note that the pin 1 and pin 8 gate terminals of both astables are tied together, and the astables are thus both activated directly by S_1 (or by an externally applied logic 0 signal).

The circuits of *Figures 5.12 to 5.14* are all non-latching types, which produce an output only when they are activated by contact switches, etc. By contrast, *Figures 5.15 and 5.16* show two ways of using the CD4001 i.c. so that it gives some form of self-latch alarm-generating action.

The *Figure 5.15* circuit is that of a one-shot or auto-turn-off generator. Here, the two right-hand gates are wired as an 800 Hz gated astable generator, and the two left-hand gates are wired as a monostable or

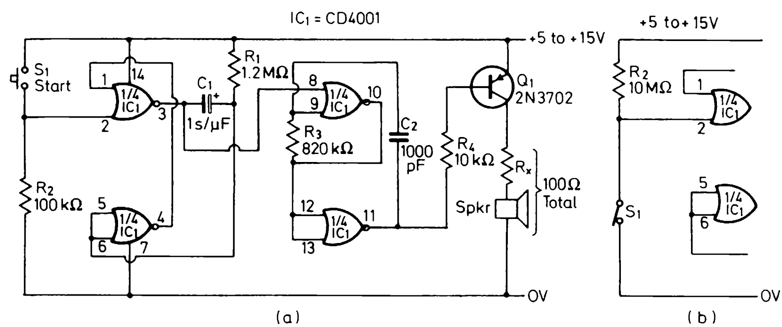


Fig. 5.15. One-shot 800 Hz alarm-call generator: (a) close to operate; (b) modification for break-to-operate

one-shot generator. The action of this circuit is such that an 800 Hz monotone alarm signal is initiated as soon as switch S_1 is momentarily operated. This alarm signal continues to be generated for a preset period, irrespective of the state of S_1, and at the end of this period the alarm signal automatically turns off. The duration of the alarm signal is determined by the value of C_1, and approximates one second per microfarad of value. Turn-off periods of several minutes can readily be obtained.

Figure 5.16 shows the circuit of a true self-latching 800 Hz alarm generator. Here, the two left-hand gates of the i.c. are wired as a manually-triggered bistable multivibrator, and the two right-hand gates are wired as a gated 800 Hz astable that is activated via the bistable.

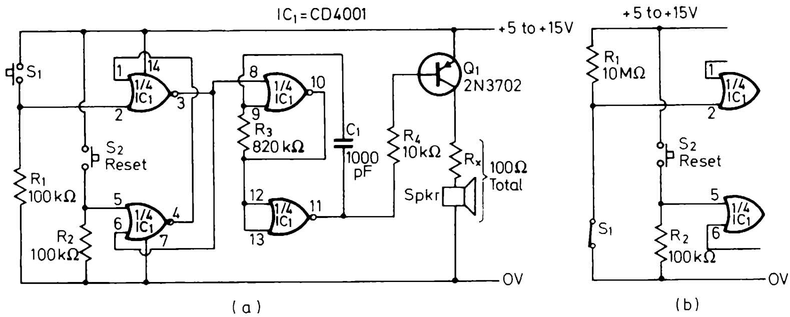


Fig. 5.16. Self-latching 800 Hz alarm-call generator: (a) close-to-operate; (b) modification for break-to-operate

Circuit action is such that the output of the bistable is normally high, so the astable is disabled and the circuit draws only a small leakage current. When S_1 is momentarily operated, a positive signal is applied to pin 2 of the i.c., so the bistable changes state and its output locks into the low state and activates the astable multivibrator. An 800 Hz tone is generated in the speaker under this condition. Once it has been activated, the circuit can only be turned off again by removing the positive signal from pin 2 and briefly closing 'reset' switch S_2, at which point the circuit resets and its quiescent current returns to leakage levels.

The *Figure 5.12 to 5.16* alarm-call generator circuits are intended for low-power operation only, and give output powers of only a few milliwatts. If desired, the power outputs of these circuits can be boosted to more useful levels by using the medium-power output-stage circuit of *Figure 5.17a*. The output power of this circuit again depends on the supply-rail and speaker-impedance values used, and may vary from 0.25 W when a 25 Ω speaker is used with a 5 V supply, to 11.25 W

when a 5 Ω speaker is used with a 15 V supply. Alternatively, the output level can be boosted to about 18 W by using the high-power output stage of *Figure 5.17b*.

The *Figure 5.12 to 5.16* circuits are designed to be permanently connected across a power supply, and to be gated on and off via electronic or switch-derived signals applied to their input-gate terminals. In some applications it may be preferred to have the circuits connected to

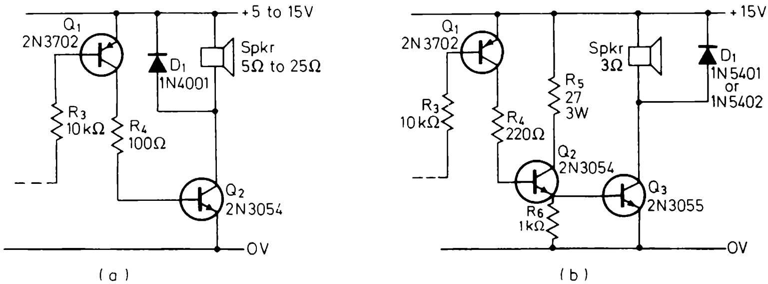


Fig. 5.17. Output power levels of Fig. 5.12 to 5.16 circuits can be boosted by using (a) medium-power (0.25–11.25 W) or (b) high power (18 W) output stage

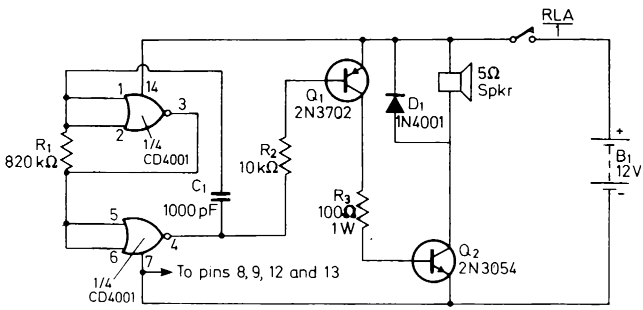


Fig. 5.18. Monotone 10 W alarm-call generator

the power-supply lines via a set of relay contacts only when the 'alarm call' function is required, and in this case the input-gate function is not needed. *Figures 5.18 to 5.20* show how the monotone, pulsed-tone and warble-tone circuits can be modified for this type of operation, each giving an output power of 10 W into a 5 Ω speaker when powered from a 12 V supply.

The *Figure 5.18* circuit gives an 800 Hz monotone output. The *Figure 5.19* circuit gives an 800 Hz pulsed tone output. The *Figure 5.20* circuit gives a warble-tone output that switches alternately between 600 Hz and 450 Hz at a rate of 6 Hz.

It was mentioned at the start of this 'alarm-call' generator section that two i.c.s have particular appeal in this type of application. The second of these is the type 555 timer i.c. Among the special attractions of this i.c. are the facts that it can be operated from a wide range of supply voltages, that it can be used in either the astable or monostable modes, that its timing periods can be controlled or modulated via an

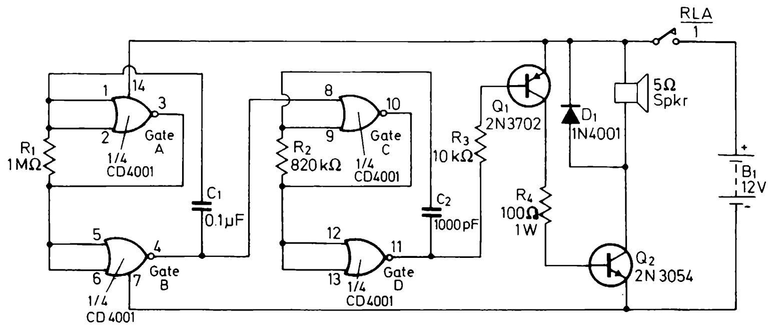


Fig. 5.19. Pulsed-outpu 10 W alarm-call generator

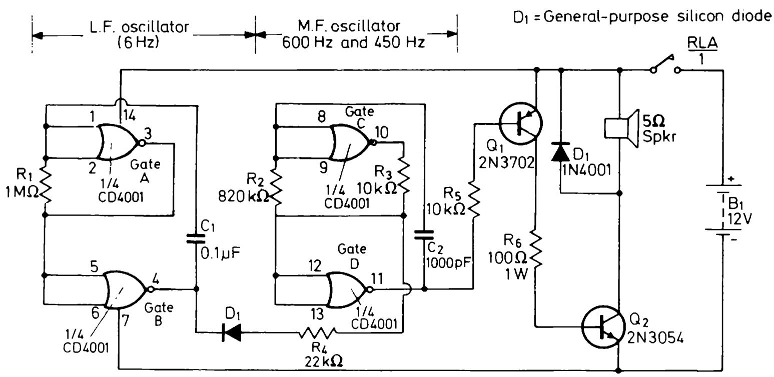


Fig. 5.20. Warble-tone 10 W alarm-call generator

externally-applied voltage, and that it is capable of directly delivering an output power of a few hundred milliwatts. *Figures 5.21 to 5.24* show some practical alarm-call generator applications of this i.c.

Each of the 555 circuits can be powered from any d.c. supply in the range 5 V to 15 V, and can be used with any output speaker impedance. Note, however, that R_x must be wired in series with speakers having impedances less than 75 Ω, and must be chosen to give a total series impedance of at least 75 Ω, to keep the peak speaker currents within

the 200 mA driving constraints of the 555 i.c. The available alarm output power of the circuits depends on the speaker impedance and supply voltage used, but may be as great as 750 mW when a 75 Ω speaker is used with a 15 V supply.

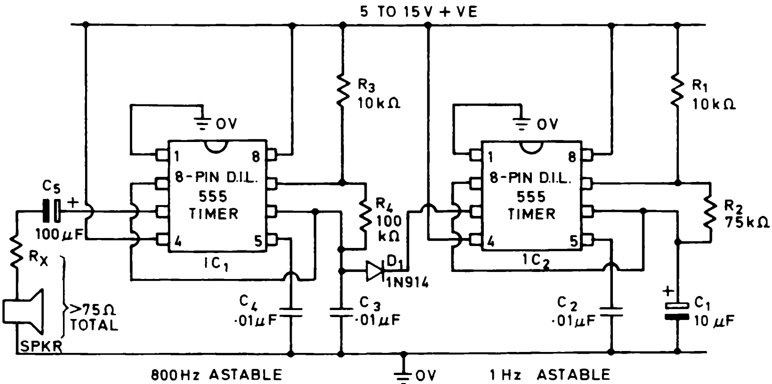


Fig. 5.21. Pulsed-tone (800 Hz) alarm-call generator

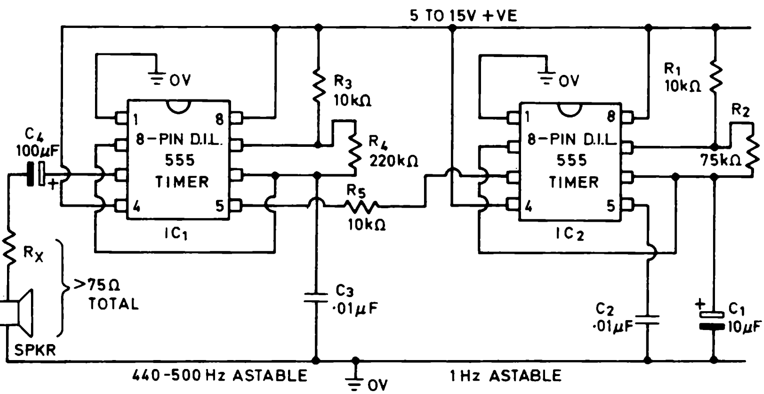


Fig. 5.22. Warble-tone alarm-call generator simulates British police siren

The *Figure 5.21* circuit is that of a pulsed-tone (800 Hz) alarm-call generator. Here, IC_1 is wired as an 800 Hz astable generator, and IC_2 is wired as a 1 Hz astable that gates IC_1 on and off once every second, thus causing the pulsed-tone output signal to be generated.

The *Figure 5.22* circuit generates a warble-tone signal that simulates the 'dee-dah' sound of a British police-car siren. Here, IC_1 is again wired

as an astable alarm generator and IC_2 is wired as a 1 Hz astable multivibrator, but in this case the output of IC_2 is used to frequency-modulate IC_1 via R_5. The action is such that the output frequency of IC_1 alternates symmetrically between 500 Hz and 440 Hz, taking one second to complete each alternating cycle.

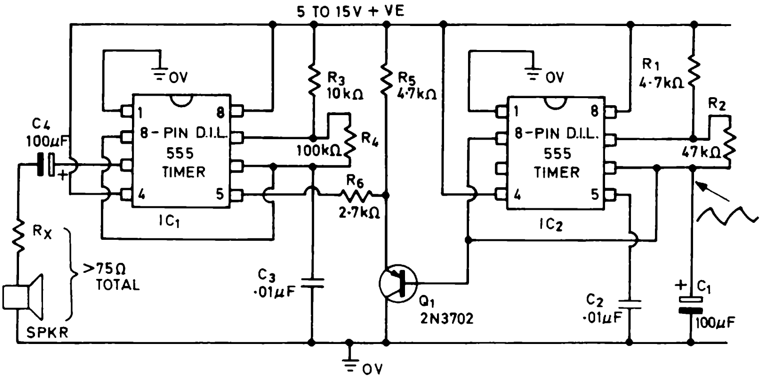


Fig. 5.23. 'Wailing' alarm simulates American police siren

The *Figure 5.23* circuit generates a 'wailing' alarm that simulates the sound of an American police siren. Here, IC_2 is wired as a low-frequency astable that has a cycling period of about six seconds. The slowly varying 'ramp' waveform of C_1 of this i.c. is fed to pnp emitter-follower Q_1, and is then used to frequency-modulate alarm generator IC_1 via R_6. IC_1 has a natural centre frequency of about 800 Hz. The circuit action is such that the alarm output signal starts at a low frequency, rises for three seconds to a high frequency, then falls over three seconds to a low frequency again, and so on *ad infinitum*.

Finally, to complete this chapter, *Figure 5.24* shows a circuit that generates a siren alarm signal that is a simulation of the 'Red Alert' alarm used in the Star Trek television series. This signal starts at a low frequency, rises for about 1.15 seconds to a high frequency, ceases for about 0.35 seconds, then starts rising again from a low frequency, and so on *ad infinitum*. The circuit action is as follows.

IC_2 is wired as a non-symmetrical astable multivibrator, in which C_1 alternately charges via R_1 and D_1, and discharges via R_2, thus giving a rapidly rising and slowly falling 'sawtooth' waveform across C_1. This waveform is fed to pnp emitter-follower Q_1, and is thence used to frequency-modulate pin 5 of IC_1 via R_6. Now, the frequency-modulation action of pin 5 of the IC_1 astable circuit is such that a rising voltage on

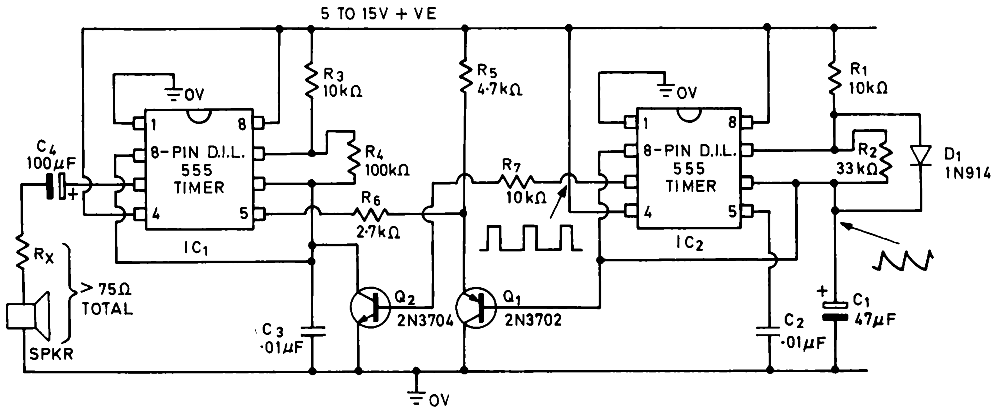


Fig. 5.24. 'Red Alert' siren alarm simulates 'Star Trek' alarm signal

pin 5 causes the astable frequency to fall, and vice versa. Consequently the sawtooth modulation signal on pin 5 causes the astable frequency to rise slowly during the falling part of the sawtooth and collapse rapidly during the rising part of the sawtooth. The rectangular pin 3 output of IC_2 is used to gate IC_1 off via npn common-emitter amplifier Q_2 during the collapsing part of the signal, so only the rising parts of the alarm signal are in fact heard, as in the case of the genuine Star Trek 'Red Alert'.

CHAPTER 6

WAVEFORM MODULATION

Generated waveforms can be modulated in a variety of ways in order to convey information or to produce special sound effects. The three best-known forms of modulation are, of course, amplitude modulation (a.m.), frequency modulation (f.m.), and frequency-shift keying (f.s.k.), but a variety of other forms of modulation, such as phase-shift keying (p.s.k.), sweep modulation and carrier keying are also used. In this final chapter we look briefly at these forms of modulation, and show a few ways of applying them to practical circuits.

Amplitude-modulation circuits

A 'carrier' waveform can be amplitude-modulated by a low-frequency 'modulation signal' by passing both signals through a non-linear device that gives an output proportional to the product of the two input signals. Semiconductor diodes and transistors are non-linear devices, and can easily be used to give amplitude modulation. Most transistor $L-C$ oscillator circuits operate in such a way that the transistor is used in the non-linear mode, and in such cases an a.m. output can be obtained by using the low-frequency modulation signal to control the emitter or the collector current of the transistor oscillator, as shown in the practical circuit of *Figure 6.1*.

The *Figure 6.1* circuit is that of a 465 kHz beat-frequency oscillator (b.f.o.), in which an external amplitude-modulating signal is fed to the emitter of Q_1 via blocking capacitor C_2. The value of emitter-decoupling capacitor C_1 is such that it presents a low impedance to the 465 kHz 'carrier' signal, but a high impedance to the low-frequency modulation

signal. Transformer T_1 in this circuit can be any 465 kHz transistor i.f. transformer. This simple circuit can be used to produce modulation depths up to about 40 per cent. The circuit can be used at frequencies other than 465 kHz by using a suitable transformer in the T_1 position.

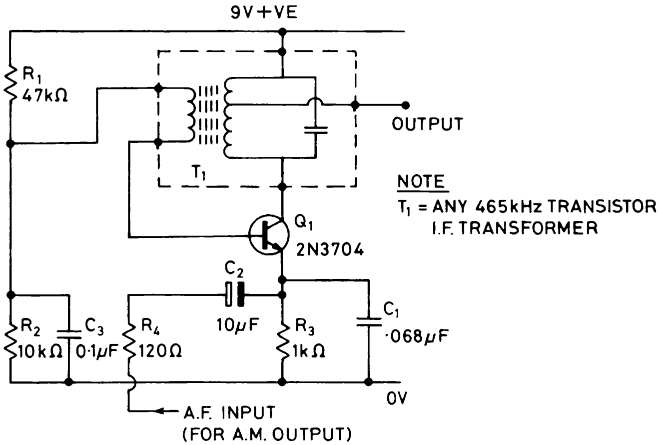


Fig. 6.1. 465 kHz b.f.o. with amplitude-modulation facility

When an oscillator circuit is directly amplitude-modulated, as in the case of the *Figure 6.1* circuit, a certain amount of frequency modulation also inevitably takes place. In cases where this frequency modulation is undesirable, the carrier signal must be amplitude-modulated at a point other than the actual oscillator stage. Where high-quality 'remote' amplitude modulation is required, the modulator can take the form of a balanced or diode-ring modulator or, if the carrier has a frequency below 50 MHz or so, it can take the form of a four-quadrant analogue multiplier integrated circuit, such as the SG3402.

The ubiquitous XR-2206 waveform-generator i.c. has a built-in four-quadrant analogue multiplier section, so this i.c. can readily be used to directly produce an a.m. signal. The pin 2 and pin 3 output-signal amplitude and phase of this i.c. can be varied by applying a bias or signal voltage to pin 1 of the 16-pin package. The output-signal amplitude is linearly controlled by variations of the pin 1 voltage about the half-supply voltage level. The output is zero when the pin 1 voltage is at the half-supply value, and rises as the control voltage increases. When the control voltage is reduced below the half-supply value the output level again increases, but its phase is reversed. This characteristic can be used to amplitude-modulate or phase-shift-key the pin 2 and 3 outputs of

the waveform generator. *Figure 6.2* shows a practical add-on amplitude-modulation facility that can be used with any of the XR-2206 sine- or triangle-wave generator circuits described earlier in this volume.

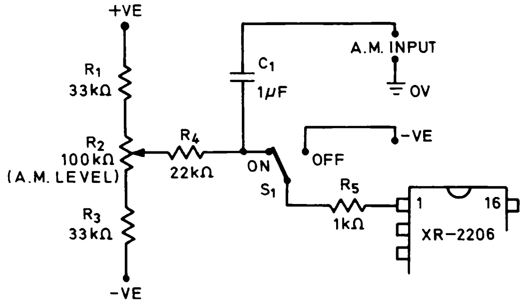


Fig. 6.2. Add-on amplitude-modulation facility that can be used with any of the XR-2206 sine or triangle generator circuits in earlier chapters

Frequency-modulation circuits

Frequency modulation can be applied to almost any type of oscillator or waveform-generator circuit by simply varying one of its frequency-determining components or parameters in sympathy with the applied modulator signal. An $L-C$ oscillator can easily be subjected to frequency modulation by wiring some form of varicap diode into its tuned circuit and applying the modulation signal to the diode. When any semiconductor diode is reverse-biased it exhibits a capacitance that varies with the applied voltage: the capacitance is greatest when the voltage is low, and is least when the voltage is high. Varicap diodes are specifically manufactured to exploit this effect, which can in fact be obtained from any diode.

Figure 6.3 shows how to use an ordinary 1N4001 silicon rectifier as a varicap diode to apply f.m. to a 465 kHz b.f.o. Here, C_2 and the diode 'capacitor' are effectively in series, and the combination is effectively wired across the T_1 tuned circuit (since the circuit's supply rails are shorted together as far as a.c. signals are concerned). Consequently the centre frequency of the oscillator can be varied by altering the capacitance of D_1 via R_4, and f.m. signals can be obtained by feeding the modulation signal to D_1 via C_3 and R_5. Note that capacitor C_2 provides d.c. isolation between Q_1 and D_1. Also note that, as in the case of the *Figure 6.1* circuit, transformer T_1 can be any 465 kHz transistor i.f. transformer.

Frequency modulation can be applied to R–C waveform generators in a variety of ways. An astable multivibrator, for example, can easily be modified so that its frequency is dependent on an externally applied d.c. voltage; the circuit then becomes a voltage-controlled oscillator (v.c.o.), and the control voltage can be modulated so that the astable produces an f.m. output signal. *Figure 6.4* shows a practical transistor astable f.m. generator of this type.

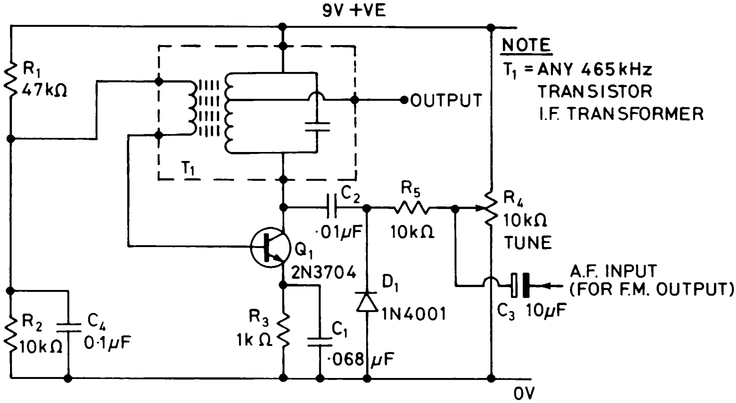


Fig. 6.3. 465 kHz b.f.o. with Varicap tuning and f.m. facility

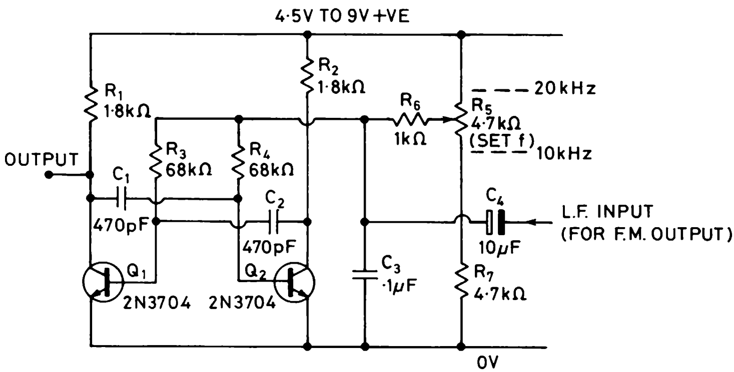


Fig. 6.4. Transistor astable circuit with variable-frequency and f.m. facility

Here, timing resistors R_3 and R_4 have their top ends taken to a variable potential divider that is wired across the supply lines, rather than directly to the positive supply rail. The circuit action is such that R_5 enables the operating frequency of the circuit to be varied over a range of roughly 2 : 1, from 20 kHz down to 10 kHz, in direct proportion to the voltage on the slider of R_5. The frequency is at a maximum

when the slider of R_5 is taken directly to the positive supply line. The astable can be subjected to frequency modulation by feeding the low-frequency modulation signal to the tops of R_3 and R_4 via C_4. The value of C_3 is chosen so that it presents a low impedance to the 'carrier' signal, but a high impedance to the modulation signal.

The XR-2206 waveform generator i.c. can readily be subjected to either frequency modulation or frequency sweeping (which is, after all, a form of f.m.). The frequency of oscillation of this i.c. is directly proportional to the total current drawn from timing pin 7 or 8 over the current range 1 μA to 3 mA. These timing pins are low-impedance points that are internally biased at +3 V with respect to pin 12. Consequently, the frequency can be varied (a) by wiring a variable current-determining resistor between pin 12 and the timing terminal, or (b) by applying a variable voltage in the range 0 V to +3 V between pin 12 and the timing terminal via a current-limiting resistor, or (c) by a combination of these two techniques. The technique outlined in (b) can be used to frequency-sweep the output signals of the XR-2206, and the technique mentioned in (c) can be used to frequency-modulate the output signals.

Figure 6.5 shows the basic connections of a simple frequency-sweep circuit that can be used to impart a 6 : 1 range of frequency coverage

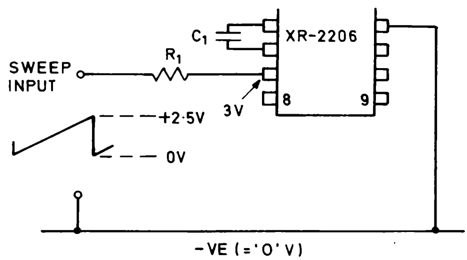


Fig. 6.5. Circuit for applying frequency sweep to XR-2206 waveform-generator i.c.; gives a 6 : 1 sweep

to the XR-2206 i.c. Here, a sawtooth frequency-sweep signal, with a peak amplitude of 2.5 V, is applied between pin 12 and the pin 7 timing terminal via limiting resistor R_1. Consequently, when the instantaneous peak value of the sawtooth voltage is zero, 3 V is developed across R_1, and the oscillation frequency is $1/RC$ Hz, as in the case of a simple resistance-controlled XR-2206 oscillator. When, on the other hand, the instantaneous peak value of the sawtooth voltage is 2.5 V, only 0.5 V is developed across R_1, and the R_1 current is only one-sixth of that of the case we have just looked at, so the frequency falls to $1/6RC$ Hz. The

frequency of oscillation is thus determined by the instantaneous value of the sweep voltage and by the R_1 and C_1 values. The frequency can, in theory, be varied over a range of at least 1000 : 1 by using this simple frequency-sweep technique.

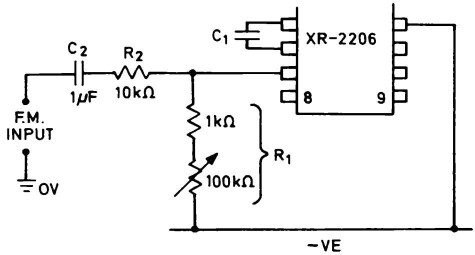


Fig. 6.6. Simple f.m. facility for the XR-2206 i.c.

Figure 6.6 shows the essential connections of a simple f.m. facility for the XR-2206 i.c. Here, in the absence of an f.m. input signal, the operating frequency is determined by R_1 and C_1, as in the case of a conventional XR-2206 oscillator. When the f.m. input signal is connected to the circuit, the f.m. input currents are added to those of R_1 via R_2, so the timing currents and thus the operating frequency of the circuit are effectively modulated by this input signal. C_2 is used to block any d.c. components between the input signal and the main timing resistor.

A weakness of the simple *Figure 6.6* circuit is that, for a given amplitude of input signal, the percentage deviation or sensitivity of the f.m. facility varies with the setting of the R_1 frequency control. This snag is overcome in the constant-sensitivity circuit of *Figure 6.7*. Here,

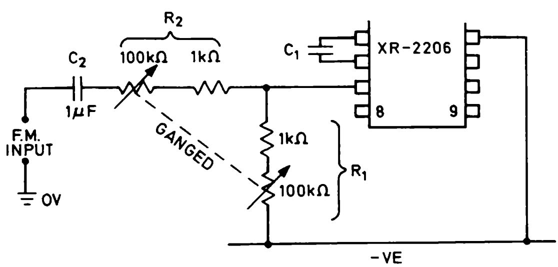


Fig. 6.7. Constant-sensitivity f.m. facility for the XR-2206 i.c.

a dual ganged pot is used with one arm connected to the R_1 frequency-determining network and the other arm connected to the R_2 f.m.-sensitivity network, so that the sensitivity is automatically adjusted to track with the frequency setting.

The type 555 timer i.c. can be subjected to frequency modulation or pulse-position modulation (p.p.m.) when it is used in the astable mode, simply by feeding a suitable modulation signal to pin 5 of the i.c., as shown in *Figure 6.8*. This modulation signal can take the form of an a.c. signal that is fed to pin 5 via a blocking capacitor, as in the case of

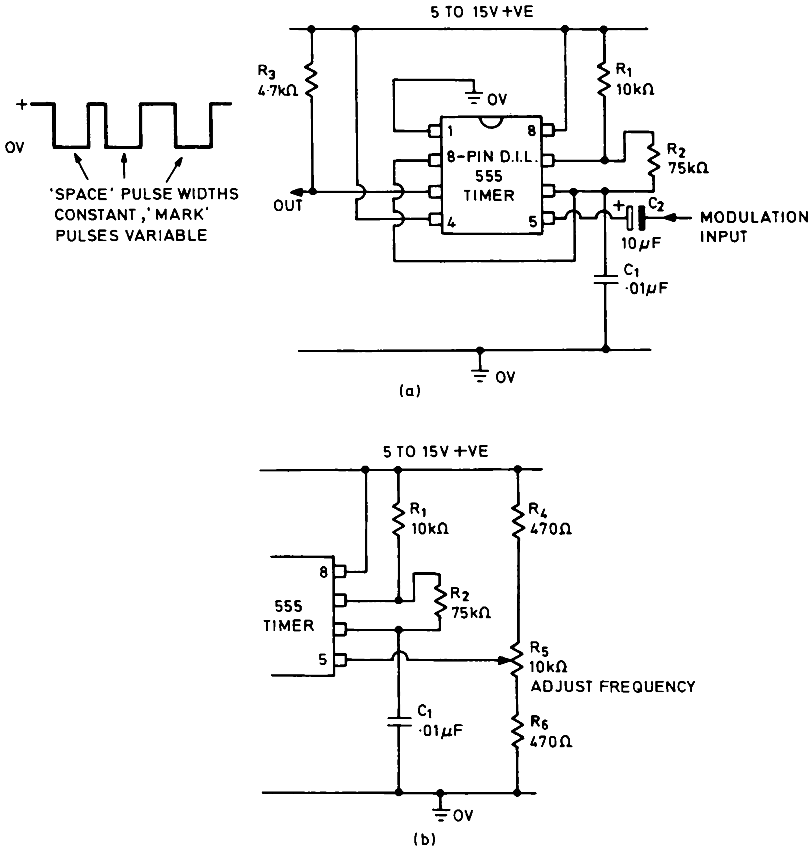


Fig. 6.8. Alternative ways of obtaining frequency or pulse-position modulation from 555 astable circuit

Figure 6.8a, or a d.c. signal that is fed directly to pin 5, as in the case of *Figure 6.8b*. The action of the i.c. is such that the voltage on pin 5 influences the width of the 'mark' pulses in each timing cycle, but has no influence on the 'space' pulses. Thus, since the signal on pin 5 influences the position of each 'mark' pulse in each timing cycle, this

terminal provides pulse-position modulation, and, since the signal influences the total period of each cycle (and thus the frequency of the output signal), the terminal also provides frequency modulation. The two circuits of *Figure 6.8* operate at nominal frequencies of about 1 kHz with the component values shown.

Frequency-shift keying circuits

Frequency-shift keying is a form of frequency modulation in which the 'carrier' switches abruptly from one frequency to another on receipt of a command or keying signal. Most oscillator circuits can be subjected to f.s.k. by simply designing them so that an alternative frequency-determining component or parameter is selected on receipt of the 'key' signal. The 'key' signal may be delivered electromechanically via a switch, or electronically via a transistor gate, etc.

The XR-2206 waveform generator i.c. has a terminal that is specifically allocated for f.s.k. use. *Figure 6.9* shows the practical connections for

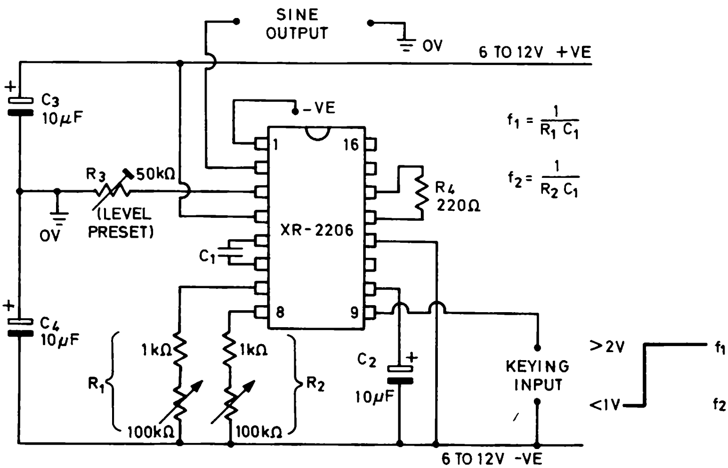


Fig. 6.9. XR-2206 split-supply f.s.k. sine-wave generator

making a split-supply sine-wave generating f.s.k. or 'warble-tone' XR-2206 oscillator. This i.c. has two alternative timing resistor pins (pins 7 and 8), and either pin can be selected by applying a suitable bias signal to pin 9 of the i.c. When the pin 9 f.s.k. input terminal is open circuit or externally biased above 2 V with respect to the negative supply rail, the pin 7 timing resistor is automatically selected and the circuit

operates at a frequency determined by R_1 and C_1. When pin 9 is shorted to the negative supply rail or biased below 1 V with reference to the negative supply rail, the pin 8 timing resistor is selected and the circuit operates at a frequency determined by R_2 and C_1. The XR-2206 i.c. can thus be frequency-shift keyed by simply applying a suitable keying or pulsing signal between pin 9 and the negative supply rail.

If required, the f.s.k. input keying signal to the XR-2206 can be referenced to the ground or zero-volts line by using the three-transistor add-on circuit shown in *Figure 6.10*. Here, with the input signal in either

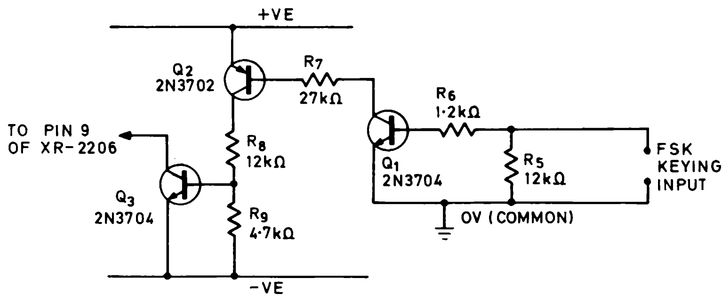


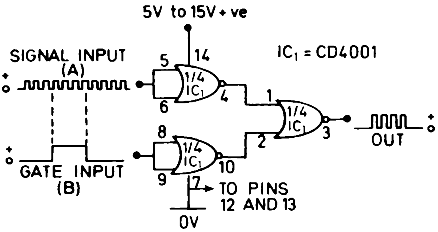
Fig.6.10. Add-on circuit enabling XR-2206's f.s.k. input keying signal to be referenced to common or ground line

the 'low' or zero state, all three transistors are cut off, so pin 9 of the i.c. is effectively open circuit, and the operating frequency of the i.c. is controlled by timing resistor R_1. When the f.s.k. input keying signal is high, Q_1 is driven on and applies bias to Q_2, Q_2 is driven on and applies bias to Q_3, and Q_3 is driven to saturation and effectively shorts pin 9 of the i.c. to the negative supply rail, so the frequency of the i.c. is controlled by R_2.

Carrier keying circuits

Carrier keying is a form of amplitude modulation in which the carrier is switched abruptly between the fully on and fully off states, and vice versa. Carrier keying can be achieved in a variety of ways. It can, for example, be obtained from any oscillator by alternately making and breaking its power-supply connections, either directly or via a slave transistor. Astable multivibrator circuits can be keyed or 'gated' on and off via an AND or an OR (or NAND or NOR) gate incorporated in one of the astable elements: *Figure 2.13a* shows an example of this type of circuit. Some circuits, such as the 555 astable ones, can be gated by

enabling or disabling their frequency-determining components: *Figures 2.19 and 2.20* show examples of this type of operation. Alternatively, the output of any waveform generator can be carrier-keyed by passing it through a suitable transmission gate. These transmission gates can be designed for either digital or linear use.



(a)

INPUT		OUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1

(b)

Fig. 6.11. (a) Circuit and (b) truth table of digital transmission-gate or carrier-keying circuit

Figure 6.11 shows the practical circuit and truth table of a COS/MOS digital transmission-gate or carrier-keying circuit. This circuit is driven by signals that are in either the logic 0 (near-zero volts) or the logic 1 (near full supply volts) state. The circuit can be powered from any d.c. supply in the range 5 V to 15 V, but care must be taken to ensure that signal and gate-input-signal voltages do not appreciably exceed the positive supply-rail voltage or fall below the level of the zero-volts rail. The action of the circuit is such that when the gate input signal is at logic 0 the output is also at logic 0, independent of the state of the signal input terminal, but when the gate input signal is at logic 1 the output follows the logic level applied to the signal input terminal. This circuit can be used to carrier-key pulse and square-wave signals with operating frequencies up to a couple of megahertz.

An excellent linear transmission-gate or carrier-keying circuit can be made by using another COS/MOS i.c., the so-called CD4016 or CD4066 quad bilateral switch. The outline and pin notations of this i.c. are shown in *Figure 6.12a*, and the simplified equivalent circuit of the device is shown in *Figure 6.12b*. As can be seen, the device effectively houses four independent electronically-controlled switches, each of which has an equivalent series resistance (R_S) when it is in the 'on' or 'closed' state. The two i.c.s differ mainly in the values of 'on' resistance that their switches offer, the CD4066 i.c. giving the better performance of the two devices.

Each of the four switches of the CD4016/CD4066 i.c. is a true bilateral device, so its input and output connections can be reversed. Each switch is provided with a control ('cont') terminal, and the device

action is such that the switch is effectively open or off when a low (logic 0) voltage is applied to its control terminal, and is closed or on when a high (logic 1) voltage is applied to its control terminal. For linear operation, the incoming signals to the switch must have positive

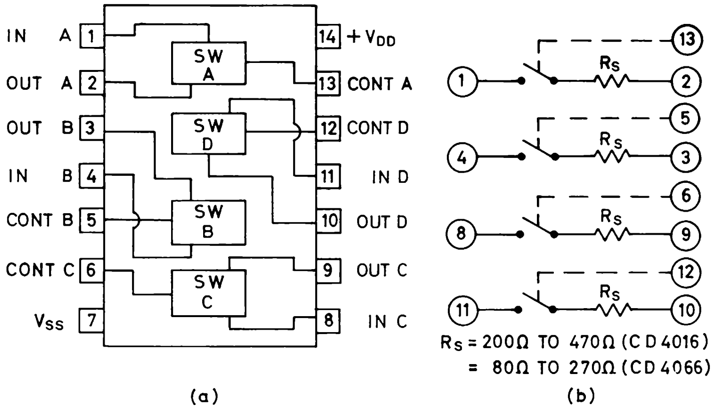


Fig. 6.12. CD4016 and CD4066 quad bilateral switch: (a) outline and pin notation; (b) simplified equivalent circuit

and negative peak amplitudes that are less than the logic 1 and greater than the logic 0 control signals respectively. The four switches in the CD4016/CD4066 package operate independently of each other, and can be used independently, or in series or in parallel, or not used at all. The input, output and control terminals of all unused switches should be connected directly to the pin-7 V_{SS} terminal of the i.c.

Figure 6.13 shows the practical circuit of a CD4016/CD4066 linear transmission-gate or carrier-keying circuit. This circuit is powered from a split supply, which can have any value in the range ±2.5 V to ±7.5 V, and makes use of switch C only. All unused switch terminals are tied to pin 7. Note in this circuit that the input and output terminals are tied to the zero-volts reference level via R_1 and R_2, and that the control voltage switches between the negative and positive supply-rail voltages.

Figure 6.14 shows how the above circuit can be modified for single-supply operation. Any supply in the range 5 V to 15 V can be used. Note in this circuit that the input and output terminals are referenced to the half-supply volts level by potential dividers R_1–R_2 and R_3–R_4 respectively to allow the maximum possible input-signal amplitudes to be handled, and to ensure that no d.c.-level shifting occurs when the switch is gated between the on and off states.

Also note that both the *Figure 6.13 and 6.14* circuits can handle input signals over the frequency range 20 Hz to 1 MHz. At frequencies above 1 MHz excessive signal breakthrough occurs between input and output. This 'breakthrough' problem can be minimised by cascading

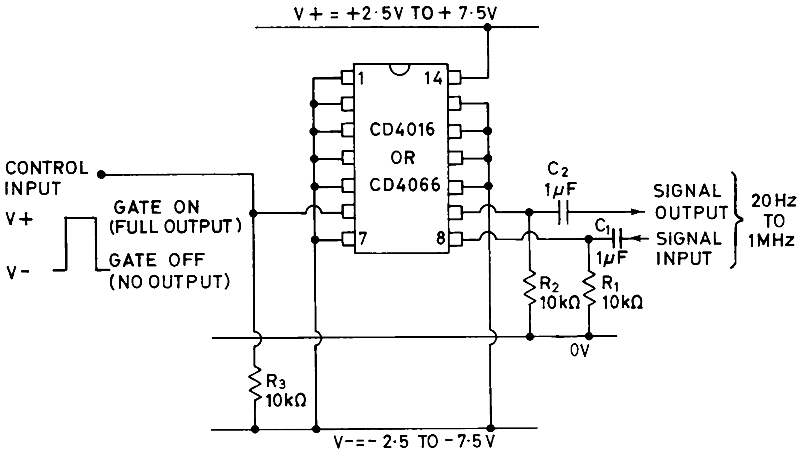


Fig. 6.13. Split-supply linear transmission-gate or carrier-keying circuit

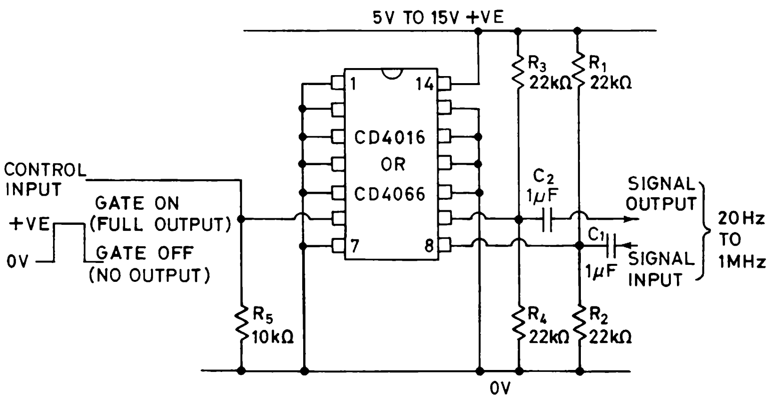


Fig. 6.14. Single-supply linear transmission-gate or carrier-keying circuit

switches from the CD4016/CD4066 package, in which case the i.c. can be effectively used at frequencies up to 10 MHz.

Finally, readers with an interest in electronic music and special-effects sound generator circuits may care to note that the circuits of *Figures*

6.13 and 6.14 are ideally suited to use in electronic organs, etc., for keying tone signals. They should also note that many of the circuits described under the headings 'amplitude modulation' and 'frequency modulation' in this chapter can be used to impart tremolo (a.m.) and vibrato (f.m.) to musical tone generators.

APPENDIX 1
SEMICONDUCTOR DETAILS

Most of the semiconductor devices used in the circuits described in this volume are well known and readily available types. In case of difficulty, however, UK readers can obtain all of them from Arrow Electronics Ltd, Leader House, Coptfold Road, Brentwood, Essex.

The 2N3702, 2N3704 and 2N3904 transistors used in many of the projects are general-purpose silicon types. In most cases they can be replaced by almost any similar types of devices having h_{FE} values better than about 100. The 2N3702 is a pnp device, and the 2N3704 and 2N3904 are npn devices.

The outlines and pin designations of all semiconductors are shown on following pages of this appendix.

The only 'rare' device referred to is the XR-2206 waveform generator i.c. A brief description of this is given below.

The XR-2206 i.c.

The XR-2206 i.c. is manufactured by Exar Integrated Systems Inc., who describe it as a monolithic function-generator chip. The device is capable of generating high-quality sine, square, triangle, ramp and pulse waveforms, at frequencies from a fraction of a hertz to several hundred kilohertz, with a minimum of external circuitry. The frequency can be swept over a 2000 : 1 range using a single control voltage or resistance. In addition, the generator can be subjected to a.m. or f.m. control, or to phase-shift or frequency-shift keying.

The XR-2206 is housed in a standard 16-pin d.i.l. package, and can be powered from either a single supply in the range 10 V to 26 V, or a

split supply in the range ±5 V to ±13 V. When used in the sine-wave generator mode, the t.h.d. of the signal is typically 2.5 per cent without adjustment, but can be reduced to about 0.5 per cent via external trimmer controls. The sine-wave output signal has a typical maximum amplitude of 2 V r.m.s. and an output impedance of 600 Ω. The frequency stability of the i.c. is excellent, being of the order of 20 ppm/°C for thermal changes and 0.01%/V for supply-voltage changes.

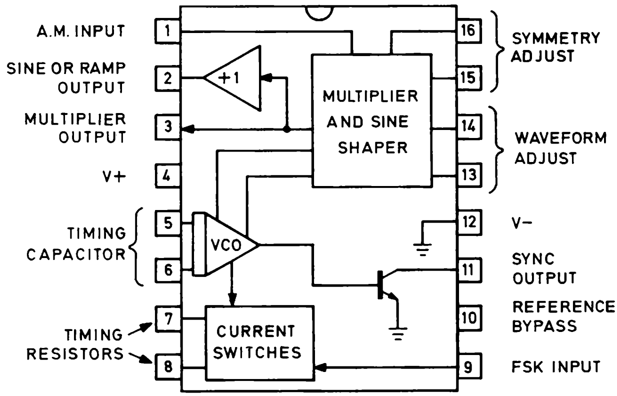


Fig. 7.1. Functional block diagram and pin connections (top view) of XR-2206 function-generator i.c.

Figure 7.1 shows the functional block diagram and pin connections of the XR-2206 i.c. The heart of the unit is a voltage-controlled oscillator (v.c.o.), which is driven via a pair of current switches. The v.c.o.'s main timing capacitor is wired between pins 5 and 6, and can have any value in the range 1000 pF to 100 μF. The v.c.o.'s main timing resistor (which controls the device's timing currents) is wired between the negative supply rail of the circuit and pin 7 or 8 of the i.c., and can have any value in the range 1 kΩ to 2 MΩ.

The frequency of oscillation, f_0, is determined by the external timing capacitor across pins 5 and 6, and by the timing resistor R connected to either pin 7 or 8. The frequency is given as $f_0 = 1/RC$ Hz, and can be varied via either R or C. For optimum thermal stability and minimum sine-wave distortion, R should have a value in the range 4 kΩ to 200 kΩ.

Either the pin 7 or the pin 8 timing resistor can be selected by applying a suitable voltage or signal to the pin 9 f.s.k.-input terminal of the i.c. If pin 9 is open circuit or connected to a bias voltage greater than 2 V, the pin 7 resistor is selected. Conversely, if pin 9 is biased below 1 V, the pin 8 timing resistor is selected. This f.s.k. facility enables the output signal to be switched alternately between two independently adjustable frequencies, to produce, for example, a warble-tone signal.

The v.c.o. section of the i.c. produces two basic waveforms simultaneously. One of these is a linear ramp, which is fed to an internal multiplier and sine shaper block, and the other is a rectangular waveform, which can be passed on to pin 11 via a built-in buffer transistor. In very simple terms, the action of the v.c.o. is such that timing capacitor C_1 first charges linearly (via a constant current set by its timing resistor) to produce a rising ramp at one output and a 'high' rectangle voltage at the other, until a certain firing voltage is reached; at this point the rectangle output switches sharply to the 'low' state, and the timing capacitor starts charging in the reverse direction, via the timing resistor constant current, to produce a falling output ramp. The ramp continues to fall until a second firing voltage is reached, at which point the rectangular output switches sharply back to its original 'high' state, and the whole timing process then repeats *ad infinitum*.

Thus the v.c.o. produces symmetrical triangle and square waveforms if the *same* timing resistor is used to control *both* charging cycles of the timing capacitor. Alternatively, if the pin 11 rectangular output waveform is shorted to the pin 9 f.s.k. terminal of the i.c., the v.c.o. automatically switches between the pin 7 and pin 8 timing resistors on alternate half cycles. This enables the i.c. to produce, simultaneously, non-symmetrical linear ramp (or sawtooth) and non-symmetrical square (or pulse) output waveforms.

The v.c.o. section of the i.c. is actually a current-controlled multivibrator, in which the timing current is controlled by the resistors connected to pins 7 and 8, or by external voltages or signals connected to these pins via suitable current-limiting resistors. This facility makes it possible to frequency-modulate or frequency-sweep the generated signals externally.

The ramp output waveform of the v.c.o. section of the XR-2206 i.c. is fed into the multiplier and sine-shaper block of the device. This block acts like a gain-controlled differential amplifier, and effectively gives a high impedance output at pin 3 and a 600 Ω buffered output at pin 2. With pins 13 and 14 open, a ramp output waveform is available at pins 2 and 3 of the i.c. With a resistance of a few hundred ohms between pins 13 and 14, the block exponentially cuts off the peaks of the ramp input signals from the v.c.o., thus producing a sine-wave output from pins 2 and 3. With suitable adjustment, the sine waveform distortion can typically be reduced to a mere 0.5 per cent.

The gain and output phase of the multiplier can be varied by applying a bias or signal voltage to pin 1 of the i.c. The output is linearly controlled by variations in the pin 1 voltage around the half-supply potential level. The output is zero when the pin 1 voltage is at half-supply value, and rises as the voltage increases. When the voltage is reduced below the half-supply value the output signal level again increases, but its phase

is reversed. This characteristic can be used to amplitude-modulate or phase-shift-key the outputs of the waveform generator at pins 2 and 3.

The effectively high output impedance of pin 3 of the XR-2206 i.c. is connected to the input of a built-in unity-gain amplifier stage, which produces a buffered 600 Ω output at pin 2. Consequently, the input signal to the buffer amplifier (and hence the output at pin 2) can be effectively varied by potential-divider action by wiring a variable resistor or impedance between pin 3 and an effective ground point. This facility can be utilised to provide simple gain control of the output, or can be used to facilitate gate keying or pulsing of the pin 2 output signal.

A final point to note about the XR-2206 i.c. is that the d.c. level at output pin 2 is approximately the same as the d.c. bias voltage at pin 3. Thus, d.c. level shifting can be applied to the pin 2 output by applying a suitable bias to pin 3. In most applications, pin 3 is biased halfway between the positive and negative supply-rail voltages. In split-supply circuits this means that the output signal swings about the zero-volts (common) line.

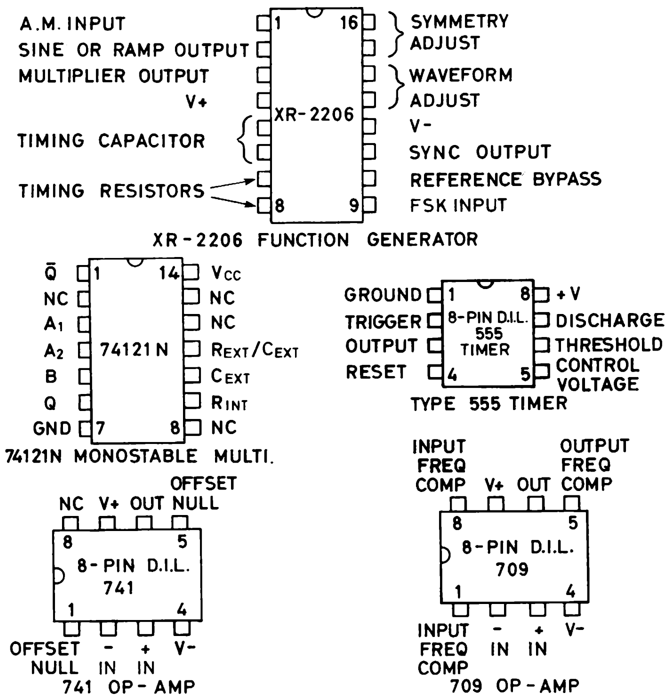


Fig. 7.2. Outlines and pin designations (top view) of i.c.s other than COS/MOS types

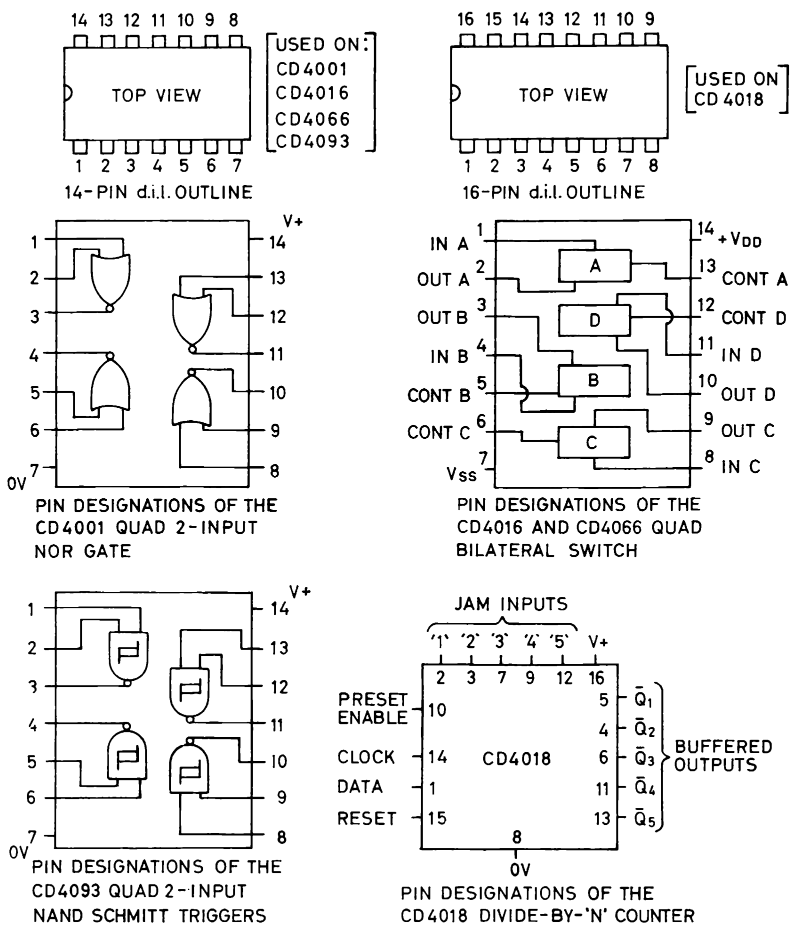


Fig. 7.3. Outlines and pin designations (top views) of COS/MOS i.c.s

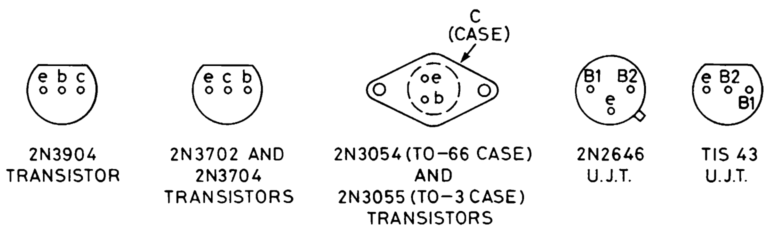


Fig. 7.4. Transistor outlines and pin designations (all viewed from below)

APPENDIX 2
DESIGN CHARTS

To conclude this volume, seven useful waveform generator design charts are presented. The methods of using these charts are as follows.

Figure 8.1: frequency–period–wavelength conversion chart

This chart enables frequency, period and wavelength to be rapidly and accurately co-related. The chart is used by simply locating the known parameter value in the appropriate column, and then reading the adjacent equivalent values of the alternative parameters.

Example. Find the period and wavelength equal to 20 MHz.

Solution. Locate 20 MHz in the centre (frequency) column, and read the equivalent period (50 ns) and wavelength (15 metres) values directly. The key of *Figure 8.1* shows how the chart can be used to cover the frequency range 0.001 Hz (1 mHz) to 1000 GHz, with appropriate changes in the period and wavelength designations.

Figures 8.2 and 8.3: symmetrical twin-T or Wien bridge component-selection charts

Two charts are presented here; between them they enable the *R* and *C* values of a symmetrical twin-T (see *Figures 1.3 and 1.4*) or Wien bridge (see *Figures 1.5 to 1.9*) network of known frequency, or the frequency for known *R* and *C* values, to be rapidly and accurately determined. The two charts are intended to be used in conjunction: *Figure 8.2* enables

the approximate parameter values to be determined, and *Figure 8.3* enables these approximate values to be translated into precise ones. The charts are used by simply laying a ruler or perspex straight edge so that it cuts the two known parameter values, and then reading the value of the third parameter at the point where its scales are cut.

Example. A 1 kHz Wien bridge oscillator is to be made using C values that are decade multiples or submultiples of 1, and with R values that are greater than 2 kΩ but less than 100 kΩ. Find the required R and C values.

Solution. Use *Figure 8.2* to find the approximate R and C values. Pivot the straight edge on the 1 kHz point of the centre scale, and rotate the straight edge so that it sweeps between the designated R limits until a qualifying C value is located. Read off the C (0.01 μF) and R (15 and a bit kilohm) values.

Use *Figure 8.3* to find the precise R values required. Lay the straight edge so that it cuts the 10 value (equal to 1 kHz) of the frequency column and the 10 value (equal to 0.01 μF) of the C column, and read off the R value of 1.59 (equal to 15.9 kΩ) at which the straight edge cuts the R column. Note that all numeric values of the *Figure 8.3* chart can be increased or decreased in decade multiples. Hence the values needed to make the 1 kHz Wien bridge oscillator are 0.01 μF and 15.9 kΩ.

Figures 8.4 and 8.5: L–C tuned circuit component-selection charts

Two charts are presented here; between them they enable the C and L values of a tuned circuit of a known frequency, or the frequency resulting from known values of C and L, to be rapidly and accurately determined. The two charts are intended to be used in conjunction: *Figure 8.4* enables the approximate parameter values to be determined, and *Figure 8.5* enables these approximate values to be translated into precise ones. The charts are used by simply laying a ruler or a perspex straight edge so that it cuts the two known parameter values, and then reading the value of the third parameter at the point where its scales are cut.

Example. Find the resonant frequency of a 200 μH coil and a 100 pF capacitance.

Solution. Use *Figure 8.4* to find the approximate frequency value. Lay the straight edge so that it cuts the 200 μH and 100 pF values, and read the frequency value as approximately 1.1 MHz.

Use *Figure 8.5* to find the precise frequency value. Lay the straight

edge so that it cuts the 2 value (equal to 200 μH) of the *L* column and the 1 or 10 value (equal to 100 pF) of the *C* column, and read off the values of 11.25/3.57 or 35.7/11.25 on the frequency column. Clearly, the 11.25 value (equal to 1.125 MHz) is the correct one that approximates 1.1 MHz. Note that all numeric values of the *Figure 8.5* chart can be increased or decreased in decade multiples in conjunction with the results of the *Figure 8.4* chart.

Figure 8.6: Timing component selector for transistor symmetrical astable multivibrators

This chart enables the necessary *R* and *C* timing component values of a transistor symmetrical astable multivibrator (see *Figures 2.3 to 2.7*) to be rapidly determined. The chart is used by laying a straight edge so that it cuts the two known parameter values, and then reading the value of the third parameter at the point where its scales are cut.

Example. A 2 kHz transistor symmetrical astable multivibrator is required. Its *R* values must be within the range 10 kΩ to 100 kΩ, and its *C* value must be a decade submultiple of 1. Find suitable *C* and *R* values.

Solution. Pivot the straight edge on the 2 kHz point of the centre scale, and rotate the straight edge so that it sweeps between the designated *R* limits until a qualifying *C* value is located. Read off the *C* (0.01 μF) and *R* (approximately 36 kΩ) values.

Figure 8.7: timing component selector for transistor monostable multivibrators

This chart enables the necessary *R* and *C* timing component values of a transistor monostable multivibrator (see *Figures 2.21 and 2.22*) to be rapidly determined. The chart is used by laying a straight edge so that it cuts the two known parameter values, and then reading the value of the third parameter at the point where its scales are cut.

Example. A transistor monostable multivibrator is required to produce output pulse widths of 100 μs. Its *R* value must be within the range 10 kΩ to 100 kΩ, and its *C* value must be a decade submultiple of 1. Find suitable *C* and *R* values.

Solution. Pivot the straight edge on the 100 μs point of the centre scale, and rotate the straight edge so that it sweeps between the designated *R* limits until a qualifying *C* value is located. Read off the *C* (0.01 μF) and *R* (approximately 14 kΩ) values.

p	f	λ
SECONDS	mHz	METRES x 10^9
ms	Hz	METRES x 10^6
μ s	kHz	METRES x 10^3
ns	MHz	METRES
ps	GHz	mm

$$f = \frac{1}{p} = \frac{300\ 000\ 000}{\lambda}$$

$$p = \frac{1}{f} = \frac{\lambda}{300\ 000\ 000}$$

$$\lambda = \frac{300\,000\,000}{f} = p \times 300\ 000\ 000$$

where p is in seconds, f is in Hz and λ is in metres

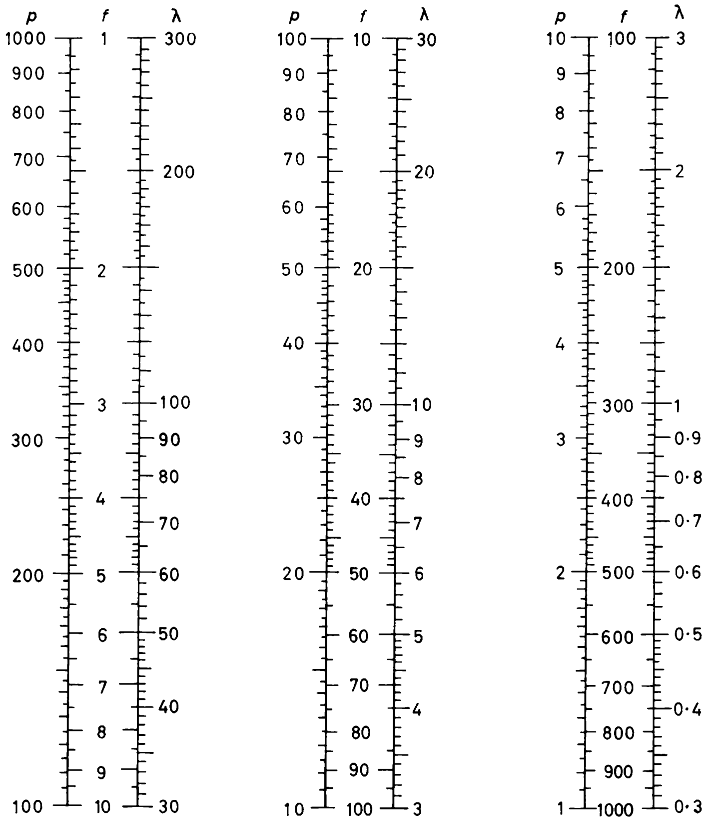


Fig. 8.1. Frequency–period–wavelength conversion chart

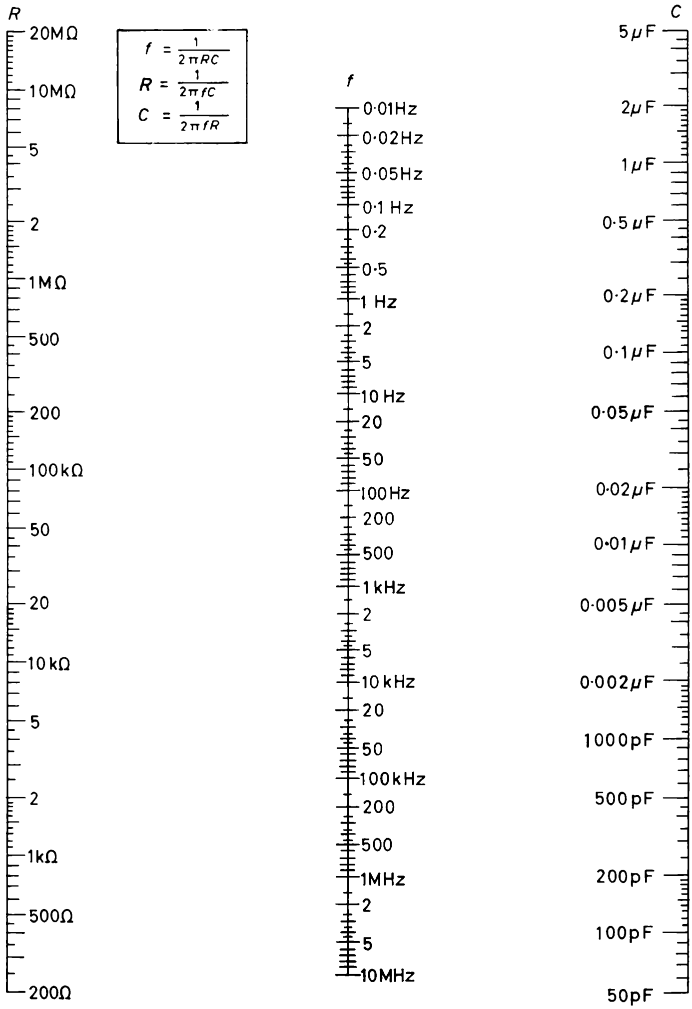


Fig. 8.2. Symmetrical twin-T or Wien bridge component-selection chart; can be used in conjunction with Fig. 8.3 to obtain greater definition

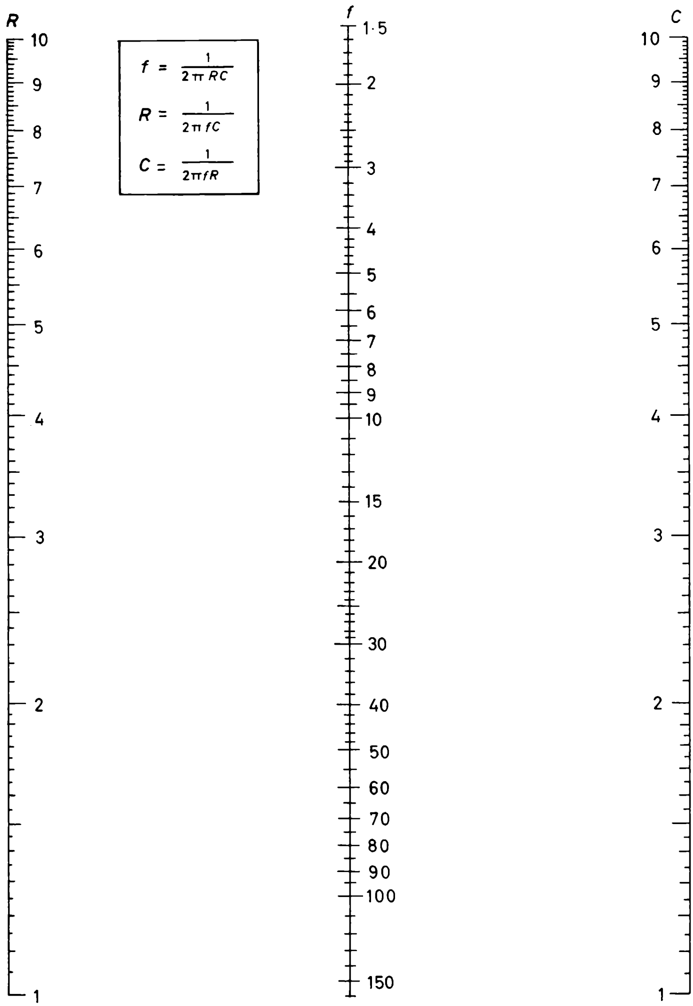


Fig. 8.3. Symmetrical twin-T or Wien bridge component-selection chart with expanded scale, to be used in conjunction with Fig. 8.2; all numerical values can be increased or decreased in decade multiples

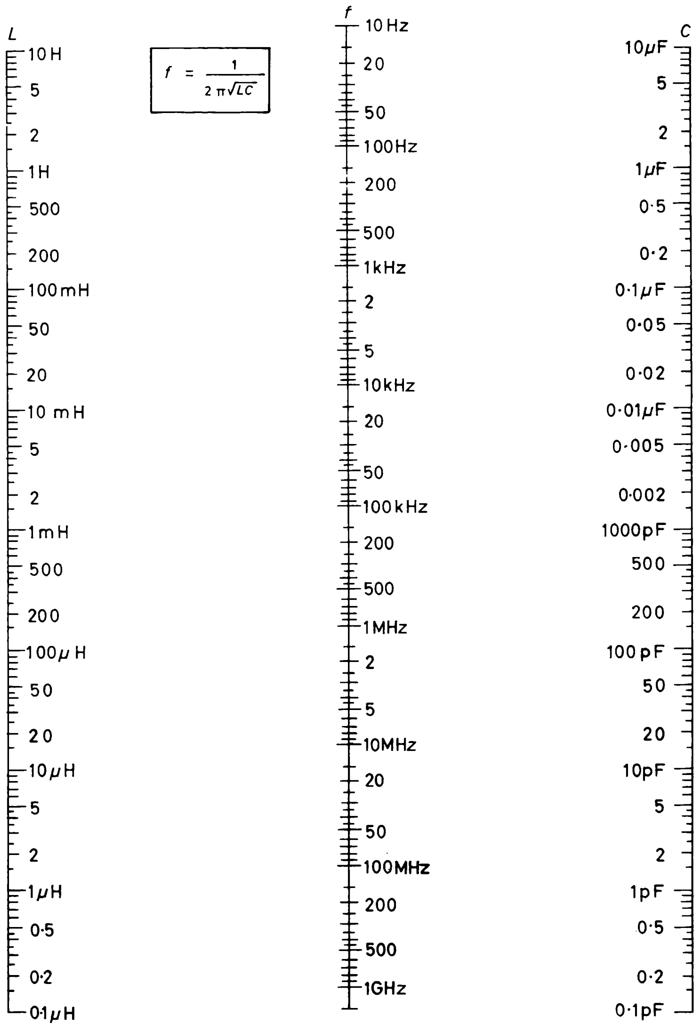


Fig. 8.4. L–C tuned circuit component-selection chart; can be used in conjunction with Fig. 8.5 to obtain greater definition

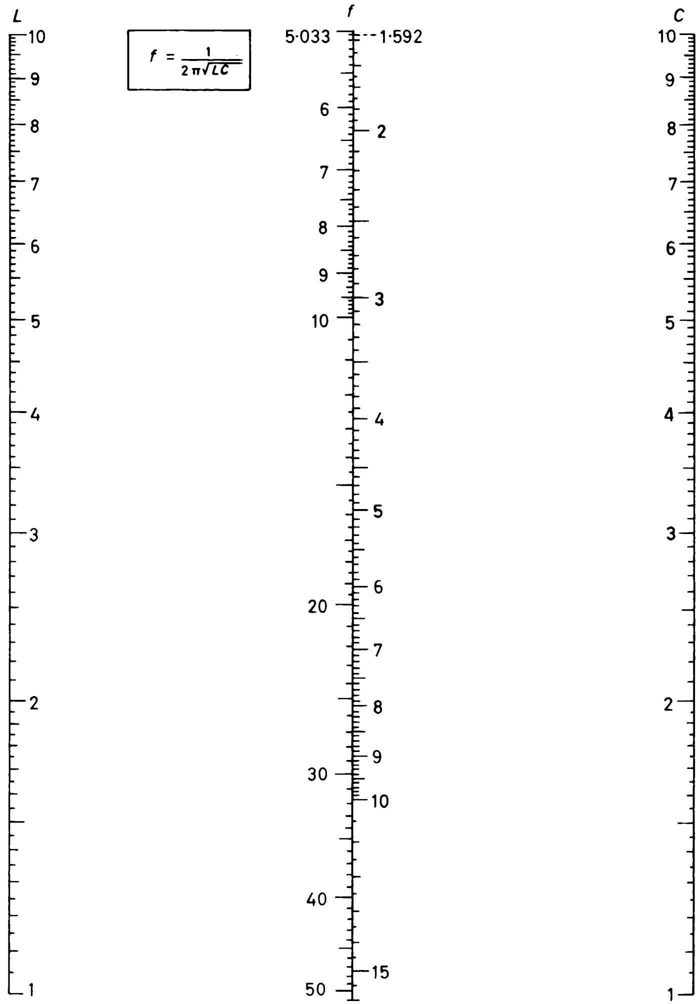


Fig. 8.5. L–C tuned circuit component-selection chart with expanded scale, to be used in conjunction with Fig. 8.4; all numerical values can be increased or decreased in decade multiples

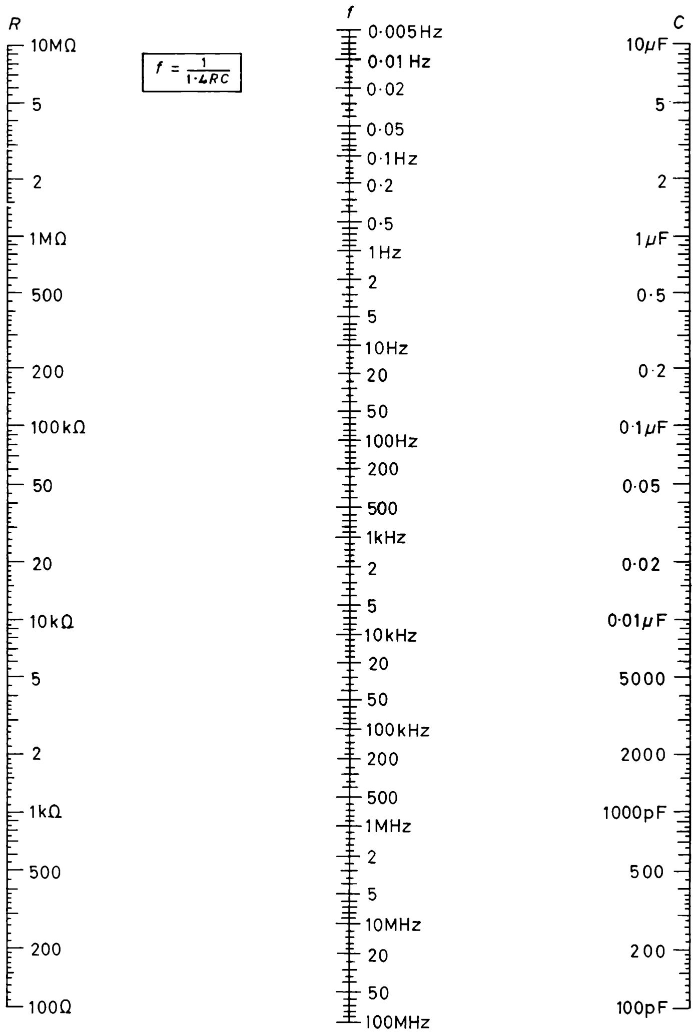


Fig. 8.6. Timing component selector for transistor symmetrical astable multivibrators

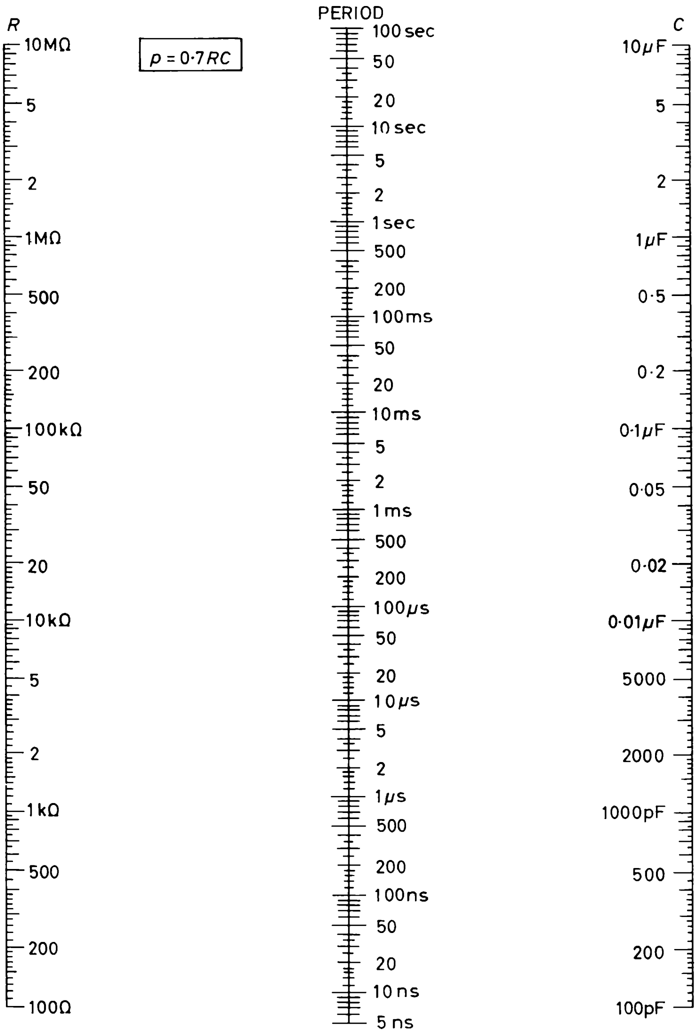


Fig. 8.7. Timing component selector for transistor monostable multivibrators

INDEX

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